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VHDL IMPLEMENTATION OF A HIGH PERFORMANCE DIGITAL UP CONVERTER USING MULTI-DDS TECHNOLOGY FOR RADAR TRANSMITTERS

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ABSTRACT:

Communication systems use the concept of transmitting information using the electrical distribution network as a communication channel. To enable the transmission data signal modulated on a carrier signal is superimposed on the electrical wires. Typical power lines are designed to handle 50/60 Hz of AC power signal; however they can carry the signals up to 500 KHz frequency. This work aims to aid transmission/reception of an audio signal in the spectrum from 300 Hz to 4000 Hz using PLCC on a tunable carrier frequency in the spectrum from 200 KHz to 500 KHz. For digital amplitude modulation
the sampling rate of the carrier and the audio signal has to be matched. Tunable carrier generation can be achieved with Direct Digital Synthesizers at a desired sampling rate. DSP Sample rate conversion
techniques are very useful to make the sampling circuits to work on their own sampling rates which are fine for the data/modulated-carrier signal's bandwidth. This also simplifies the complexity of the sampling circuits. Digital Up Conversion (DUC) and Digital Down Conversion (DDC) are DSP sample rate conversion techniques which refer to increasing and decreasing the sampling rate of a signal respectively.

Keywords: Power Line Carrier Communication, Digital Down-Counter, Digital Up-Counter, Application Specific Integrated Circuit, Multi-VDD, TSMC **I. INTRODUCTION**

This paper focuses on Design and ASIC Implementation of Digital up-converter and Down converter for communication applications at 65nm technology. Digital up-conversion and down-conversion are well known sample rate conversion processes in Digital Signal Processing. These techniques are widely used for converting a baseband signal to band pass signal and viceversa to enable the transmissionand reception. For the baseband signal to be transmitted, it needs to be modulated on to an IF/RF carrier frequency. Nyquist theorem says the sampling rate shall be at least twice the highest frequency component. Hence the base band signal, whose sample rate might be very less compared to IF/RF carrier signal sampling rate, needs to have the sampling rate to match the IF/RF carrier signal sampling rate. It's the reverse process with respect to receivers. In case of receivers the sample reduction helps to reduce the processing

complexity of the received baseband signal. In simple, down conversion can be defined as removing samples (also called as Decimation) and generating new samples by virtue of adding zeroes (also called as Interpolation) and interpolate the new samples. Depending on its flexibility, small size and low development costs, digital radar transmitter is widely used in the field of radar signal processing. The traditional radar signal transmitting process includes the generation of the base-band signal, modulated to the intermediate frequency, digital-to-analog conversion, modulated to a radio frequency and antenna transmits. Wherein the steps of generation of the base-band signal, modulated to the intermediate frequency and digital-to-analog conversion are implemented by digital radar transmitter. Fig.1 shows the traditional digital up-conversion process.

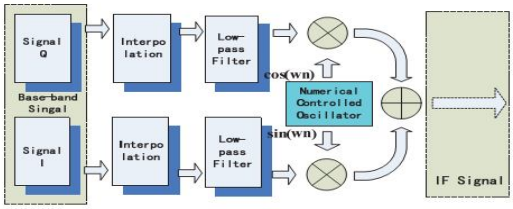


Fig.1 Traditional digital up-conversion process

Nowadays, with the demand for high performance and functionality digital radar transmitter, especially the increasing requirements on resolution and real-time system in imaging radar, the large bandwidth base-band signals have been put to use. At the same time, in order to make the digitizing hardware to meet the requirements, ultra high-speed ADC / DAC and digital processing chip must be used which will face a lot of challenges both in technics and costs. In order to take advantage of the limited hardware resources to achieve higher indicators of digital radar transmitter, this paper pays attentions on the critical multi-DDS technology in high-performance digital conversion. And it implements this algorithm on FPGA hardware

accuracy also improved. DDS technology platform. High-efficient digital up-conversion processing which is based on multi-DDS technology is shown in Fig.2.

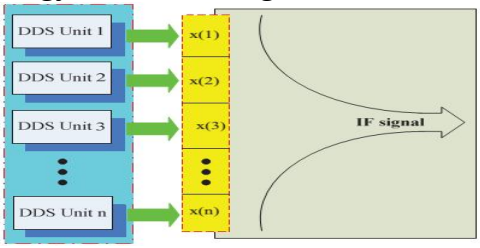


Fig.2 High-efficient digital up-conversion processing **DESIGN SPECIFICATIONS**

Functional and technology specifications of DUC and DDC designs are described in this section.

DUC

The up conversion system gets its input from anADC with 14-bit resolution, 0-5V range and a sampling frequency of 64 KHz. The input signal spectrum is from 300 to 4000Hz. The input signal has to be up-sampled by 20 and get mixed with a carrier signal ranging from 200 KHz to 500 KHz. The Direct Digital Synthesizer which generates the carrier signal is also expected to be part of the up-sampling system.

DDC

The down conversion system gets its input from an ADC with 14-bit resolution, 0-5V range and a sampling frequency of 1.28 MHz. The input signal spectrum is from 200 KHz to 500 KHz. Demodulation is expected to be part of the down conversion system. Hence the input signal is expected to be mixed with a carrier signal to generate the baseband signal. The baseband signal then has to be decimated by 20 to get the sample rate of 64 KHz.

II.MULTI-DDS TECHNOLOGY

The direct digital synthesis (DDS) technology is a new type of frequency synthesizer technology which developed on the basis of the direct analog synthesizer (DAS) and direct digital waveform synthesis technology (DDWS). It draws advanced digital signal processing theory and methods into signal synthesis field. By this way, conversion speed can be guaranteed and synthesized signal

utilizes continuous phase transformation to generate signal with high frequency resolution, low phase noise and low spurious. Owing to these advantages, traditional digital up-conversion process typically uses the DDS technology to generate a required base-band signal. There are two conventional implementations of DDS technology. One of them uses a dedicated DDS chip and another uses the field programmable gate array (FPGA) to achieve the goal. The dedicated DDS chips are simple to implement, but they are not flexible enough to complete some projects. And the use of FPGA can achieve more efficient DDS programs.

DDS Unit Principle

Direct digital synthesizer uses a lookup table to generate sine and cosine signals. And since most of the signals can be decomposed into a number of sine and cosine signals, theoretically, the DDS unit can achieve signals with arbitrary waveform.Fig.3 shows the basic structure of single DDS unit

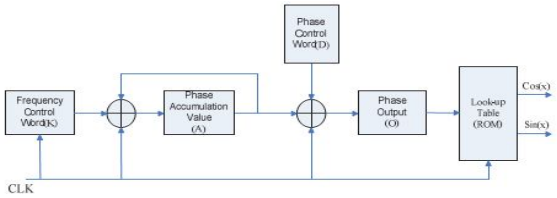


Fig.3 Basic structure of single DDS unit

DDC ASIC architecture as in Figure 8 is similar to that of shown MATLAB software mode in Figure 4; however the demodulation mixer is added prior to the decimation.

The DDS is programmable and generates the carrier frequency between 200 KHz to 500 KHz. A high pass filter immediately follows the constant frequency mixer to select the upper band (carrier + signal frequency) output from the mixer. Another change in the system is that compensation filter doesn't implement any decimation; the CIC decimation filter itself implements decimate by 20 function.

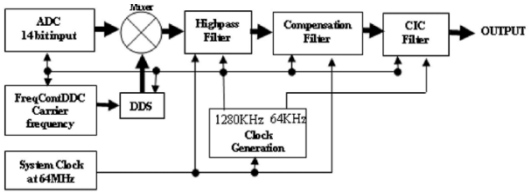


Fig 4. DDC ASIC Architecture

Multi-DDS Algorithm

Seen by the sampling theorem, when system clock is CLK, the highest frequency that a DDS can generate is 2 CLK÷ 2. If the higher frequency is required with the same clock, Multi-DDS technology supports a high-efficient solution. N channel parallel DDS units work in the clock of CLK can produce a signal with the frequency of 2 NCLK÷ < Hz. The structure of Multi-DDS is shown in Fig.5

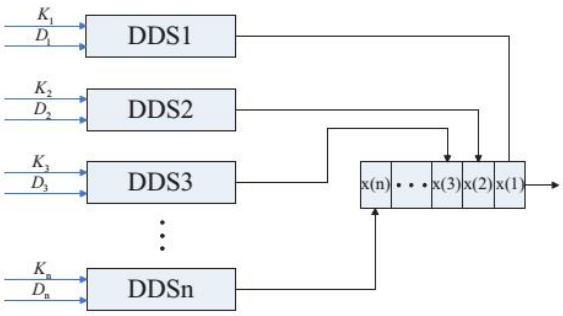


Fig.5 Structure of Multi-DDS

III. Implementation of Multi-DDS Algorithm

In this paper, the hardware platform is based on Virtex4SX55 FPGA from Xilinx Inc. The FPGA works at 150MHz, and utilizes the four-phase DDS technology to achieved an IF signal with 100MHz bandwidth.

The center frequency of LFM signal is 200MHz and the sampling rate is up to 600MHz. In this scheme, four DDS IPCores are called and every DDS unit works at streaming mode. The structure of DDS IPCore is shown in Fig.6

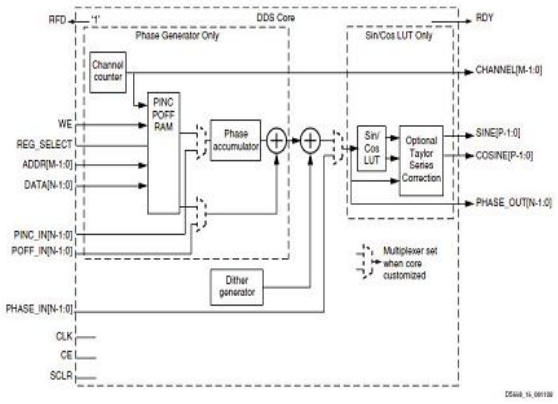


Fig.6 Structure of DDS IPCore

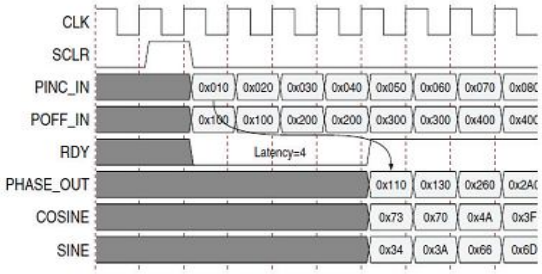


Fig.7 Timing diagram of streaming mode

1) Parameter Description:

a) Spurious Free Dynamic Range(SFDR)

Due to the constraints imposed by limited bit width of the digital signal, the phases information to LUT exist truncated bit error. And when it responses to the output signal, the impact called stray. Spurious Free Dynamic Range represents the difference between the target signal and the largest spurious peak, which is expressed by dB. In order to get greater SFDR, a larger LUT is usually used. That also consumes more storage space. The relationship between bit width of LUT and SFDR can be expressed by

$$N = \frac{SFDR}{6}$$

b) Frequency resolution(FR)

Frequency resolution equals the minimum frequency that can be distinguished from output signal. It is expressed by

$$\Delta f = \frac{f_{clk}}{2^m}$$

2) ParameterSelection

The selection of parameters is decided by the demand of SFDR and FR. In this paper, considering the impact on the amount of ost-processing calculation, we chose a 14bits output. And other parameters are shown in the table.

Signal	Clock	Bandwidth	Sampling rate	Center frequency
Chirp	150MHz	100MHz	600MHz	200MHz
Output width	Phase width	Theoretical SFDR	Theoretical FR	Sweep time
14bit	31bit	78 dB	0.07Hz	12um

IV.SIMULATION RESULTS

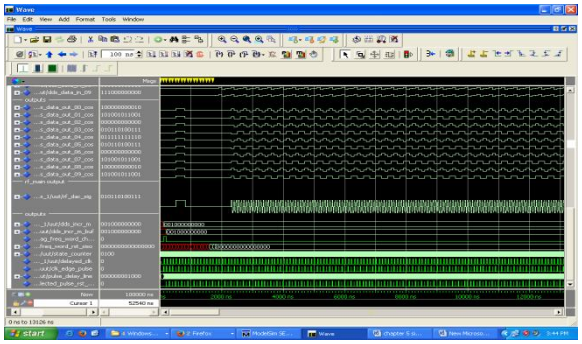
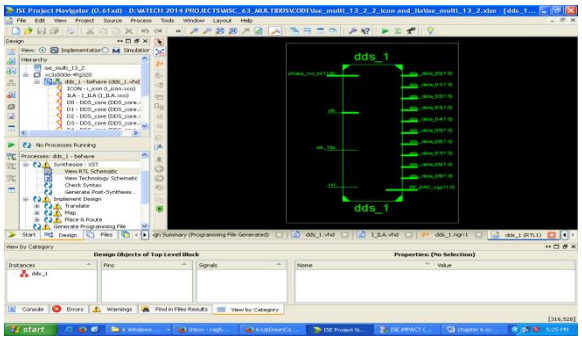


Fig 8.Simulation outputs of multi dds

RTL SCHEMATIC:



V. CONCLUSION

An efficient digital conversion process has been by researched using Multi-DDS technology which based on parallel processing, a large bandwidth signal can be produced at conditions of a lower hardware clock. Besides that this solution

eliminates the need for filtering and modulation Process and directly generates IF signal. The program has been implemented in FPGA hardware platform and achieved very good results

REFERENCE

[1] Xinsheng Zhang.FPGA Design of a High-efficiency Flexible Digital Up-converter [J]. Microcomputer & applications, 2010

[2] Zhiyong Huo.Research on Radar LFM Signal Generation System Based on DDS [J].Shanxi: Xi'an University of Electronic Science and Technology, 2004, 19(2).

[3] Xutian Liu Design of Digital Up-converter Based on FPGA [D] Shenyang: Northeastern University, 2009.

[4] Iwabuchi, M., Sakaguchi, K., Araki, K., "Study on multi-channel receiver based on polyphase filter bank," Proceedings of the 2ndInternational Conference on Signal Processing and Communication Systems, 2008, pp. 1-7.

[5] Destraz, B., Louvrier, Y., Rufer, A., "High Efficient Interleaved Multi-channel dc/dc Converter Dedicated to Mobile Applications," Proceedings of 41st lAS Annual Meeting. Conference Record of the 2006 IEEE Industry Applications Conference, 2006, pp. 2518 - 2523.

[6] Xilinx Inc. vertex_4userguides 2008.12.

[7] Xilinx Inc. LogiCORE IP DDS Compiler v4.0 2011.3.