INTERNATIONAL JOURNAL OF RESEARCH
In Advanced Engineering Technologies

Volume 2, Issue 1 SEP 2014

STUDY AND ANALYSIS OFSUBMULTILEVEL INVERTER TOPOLAGY FOR CASCADED MULTILEVEL INVERTER

PUTTA MAHESWARA

M.Tech scholar,Sri Sai Institute of Technology and Sciences in Rayachoti, KadapaAndhra Pradesh, India

M.VIJAYA KUMAR

Assistant Professor of EEE department Sri Sai institute of technology and science, Rayachoti, Kadapa, Andhra Pradesh, India

V.PRATAPARAO

Assistant Professor and HOD of EEE department Sri Sai institute of technology and science, Rayachoti, Kadapa, Andhra Pradesh, India

ABSTRACT: Multilevel inverters produce a staircase output voltage from DC voltage sources. Multilevel converters have many advantageous features over the conventional two-level topologies including capability of handling high-voltage high-power, improved output voltage quality etc. Requiring great number of semiconductor switches is main disadvantage of multilevel inverters.

This is partly because of high-quality output waveform of multilevel inverters in comparison with two-level inverters. In this paper, initially a new topology for sub multilevel inverter is proposed and then series connection of the sub multilevel inverters is proposed as a generalized multilevel inverter. The proposed multilevel inverter uses reduced number of switching devices. Special attention has been paid to obtain optimal structures regarding different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources, etc. The proposed multilevel inverter has been analyzed in both symmetric and asymmetric conditions. The validity of the proposed multilevel inverter is verified withsimulations using MATLAB/SIMULINK.

INTRODUCTION

Multilevel converters as a popular sort of power-electronic converters have been widely investigated in recent years. A typical multilevel converter uses power-electronic switches and dc voltage sources to generate a multilevel output voltage.

Multilevel inverters include an array of power semiconductors and dc voltage sources, the output of which generate voltages with stepped waveforms [1]. In comparison with a two-level voltage-source inverter (VSI), the multilevel VSI enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference [2]. By increasing the number of levels in the multilevel inverters, the output voltages have more steps in generating a staircase waveform, which has a reduced harmonic distortion. However, a larger number of levels increase the number of devices that must be controlled and the control complexity [3]. There are three well-known types of multilevel inverters [4], [5]: the neutral point clamped (NPC) multilevel inverter, the flying capacitor (FC) multilevel inverter, and the cascaded H-bridge (CHB) multilevel inverter. The NPC multilevel inverter, also called diode-clamped, can be considered the first generation of multilevel inverter introduced by Nabae et al. [6] which was a three-level inverter. The three-level case of the NPC multilevel inverters has been widely applied in different industries. Unlike the NPC type, the FC multilevel inverter offers some redundant switching states that can be used to regulate the capacitors voltage. However, the control scheme becomes complicated. Moreover, the number of capacitors increases by increasing the number of voltage levels.

The CHB multilevel inverters use series-connected H-bridge cells with an isolated dc voltage sources connected to each cell. The CHB multilevel inverters can be divided into two groups from the viewpoint of values of the dc voltage sources: the symmetric and the asymmetric topology. In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the

topology good modularity. However, the number of the switching devices rapidly increases by increasing the number of output voltage level. In order to increase the number of output voltage level, the values of the dc voltage sources are selected to be different, these topologies are called asymmetric [7], [8]. The CHB multilevel inverters have been industrially employed in several applications fields such as pump, fans, compressors, etc. In addition, they have recently been proposed for other applications like photovoltaic power-conversion system and wind power conversion [9]. The topologies discussedpreviously are the conventional topologies. Many other multilevel inverter topologies have been introduced in recent years. One of the topologies is the modular multilevel inverter [10].

This topology is simpler than the cascaded four-switch H-bridge-based inverter and has several advantages, such as modular extension to any number of levels and redundancy [11]. However, the topology does not consider reduction in the number of components used. Other multilevel inverter topologies have been introduced in [12]–[15]. The multilevel inverter presented in [15] is based on symmetric topology and uses series/parallel connection of the dc voltage sources. This topology uses lower number of switches in comparison with the symmetric CHB multilevel inverter. The topologies presented in [12] and [13] consider reduction in the components.

These topologies are basically based on asymmetric topologies; hence, the used dc voltage sources have different values.However, the number of switching devices still remains high in these topologies. A nine-level activeNPC inverter has beenpresented in [16] which is the modification of the standard active NPC converter. Nami et al. [17] present a hybrid multilevel inverter using the CHB and the diode-clamped topology. This paper proposes a new multilevel inverter topology using series-connected submultilevel inverters. The proposed multilevel inverter uses reduced number of switches. Initially, the proposed submultilevel inverter is described and then the series connection of them to form a multilevel inverter is discussed. The optimal structures of the proposed multilevel inverter regarding several factors (e.g., number of switches, number of dc voltage sources, standing voltage on the switches, etc.) are also obtained.

The power loss of the proposed topology is calculated. Afterward, the proposed multilevel inverter is compared with other multilevel inverter topologies considering the number of switches. A design example is then given which is used for simulation study.

II.PROPOSEDMULTILEVEL INVERTER

A. Proposed Sub multilevelInverter:

The proposed sub-multilevel inverter is shown in Fig.1 as depicted; the topology consists of n dc voltage sources. In general, the dc voltage sources can have different values.

However, in order to have equal voltage steps, they are considered to be the same and equal to Vdc. Each submultilevel inverter consists of n + 2 switches. Some of the switches are unidirectional and the others are bidirectional. The unidirectional switches consist of an insulated gate bipolar transistor (IGBT) with an antiparallel diode. The switches S1,S'1,S (n+2)/2, and S' (n+2)/2 are unidirectional and the other switches are bidirectional; hence, they have to withstand both positive and negative voltages. For instance, when S(n+2)/2 is turned ON, the voltage Vdc is on the switch Sn/2 , and if the switch S(n−2)/2 is turned ON, the voltage equal to −Vdc is on the switch Sn/2 .

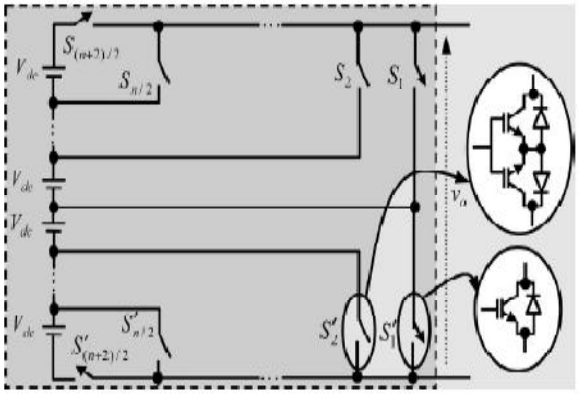

Fig. 1. Proposed generalized sub multilevel inverter.

The same conditions are valid for the other switches. Therefore, the switches have to withstand both positive and negative voltages. In addition, the switches have to conduct backward current that is as a result of inductive characteristic of the load. It can be concluded that the switches must be bidirectional. There are several circuit configurations for bidirectional switches. In this study, the common emitter topology is used as it needs one gate driver for a switch. Considering the types of the switches, 2n IGBTs are required in the proposed submultilevel inverter. It is worth mentioning that the number of the antiparallel diodes is equal to the number of IGBTs. The proposed submultilevel inverter can only generate zero and positive voltage levels. The zero output voltage is obtained when the switches S1 and are turned ON simultaneously. The other voltage levels are generated by proper switching between the switches. Table I shows the states of the switches for each output voltage value. In this table, 1 means that the corresponding switch is turned ON and 0 indicates the OFF state.

TABLE I
OUTPUT VOLTAGES FOR STATES OF SWITCHES

state	Switches states									v_0
	s_1	s_1'	s_2	s_2'	...	$s_{n/2}'$	$s_{n/2}$	$s_{(n+2)/2}$	$s_{(n+2)/2}'$	
1	1	1	0	0	...	0	0	0	0	0
2	0	1	1	0	...	0	0	0	0	v_{dc}
3	0	0	1	1	...	0	0	0	0	$2v_{dc}$
:	:	:	:	:	...		:	:	:	:
n-1	0	0	0	0	...	1	1	0	0	$(n-2)v_{dc}$
n	0	0	0	0	...	0	1	0	1	$(n-1)v_{dc}$
n-1	0	0	0	0	...	0	0	1	1	nv_{dc}

Considering Fig. 1, for each value of the output voltage of submultilevel inverter, two switches must be turned ON, one from the upper switches and the other from the lower switches. For example, to get output voltage of Vdc, the switches and S2 are turned ON. In order to obtain the output voltage of (n−1) Vdc, the switches Sn/2 and S' (n+2)/2 should be turned ON.

Considering Fig. 1, the following equations can be written:

(1)

(2)

(3)

(4)

Where, Nswitch,sub, Ndriver,sub, NIGBT,sub, and Nsource,sub are the number of switches, number of switches drivers in one submultilevel inverter, number of IGBTs in one submultilevel inverter, and number of dc sources in one submultilevel inverter, respectively.

For the proposed typical submultilevel inverter (see Fig. 1), the standing voltage on the switches is calculated. A switch experiences different off-state voltages in different switching combinations. Among these off-state voltages, the highest voltage is considered to be the standing voltage of the switch. This can be a criterion for voltage rating of the switch. For example, in Fig. 1, the switch S1 experiences the maximum off-state voltage when the switch S(n+2)/2 is turned ON that is equal to (n/2)Vdc. For the switch S2, the standing voltage is (n/2 − 1)Vdc. For the switches S_ 1 and S_ 2, the standing voltage is equal to (n/2) Vdcand (n/2 − 1)Vdc, respectively. This calculation can be done for any switch in the submultilevel inverter. The standing voltage for the submultilevel inverter is sum of all standing voltage on the switches in their off state [12]. For a submultilevel inverter including n dc voltage sources, the standing voltage on the switches depends on n and whether it is odd or even. For different n, the standing voltage on the switches of i^{th} submultilevel inverter (Vstand, i) can be obtained by (5), shown at the bottom of the next page.

B. Proposed Generalized Multilevel Inverter

The proposed submultilevel inverters can be connected in series to achieve the desired voltage and number of voltage levels. Fig. 2 shows m sub multilevel inverters in series. Each submultilevel inverter has n dc voltage source. The dc voltage sources in each submultilevel inverter are equal.

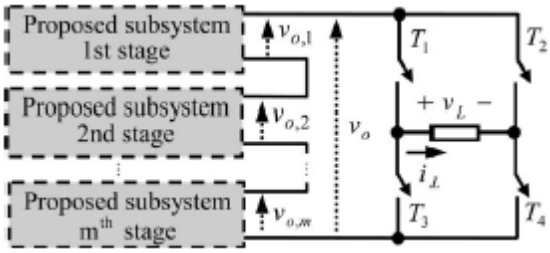

Fig. 2. Proposed general multilevel inverter using series connection of m proposed submultilevel inverters; each one has n dc voltage sources.

The output voltage of the submultilevel inverters (and series connection of them) is always positive or zero. To operate as an inverter, it is necessary to change the voltage polarity in every half cycle. For this purpose, an H-bridge inverter is added to the output of the series connected submultilevel inverters.

It is important to note that the switches of the H-bridge must withstand higher voltage. This should be considered in the design of the inverter. However, these switches are turned ON and OFF once during a fundamental cycle. So, these switches would be high-voltage low-frequency switches.

Considering that the multilevel inverter shown in Fig. 2 includes m submultilevel inverter (using (1)–(4) and considering the H-bridge part), the following equations can be written:

(6)

(7)

(8)

(9)

Where Nswitch, Ndriver,NIGBT, and Nsource are the number of switches, number of switches drivers (which is equal to number of switches), number of IGBTs, and total number of dc sources, respectively.

Considering (6) and (8), in general, the number of IGBTs is not equal to the number of switches in the proposed multilevel inverter; hence, some of the switches are bidirectional (which is considered as one switch) and consist of two IGBTs. The proposed topology can be extended to three-phase systems using three single-phase units.

Like the other multilevel converters, the switches cannot be shared between the phases, and therefore, three single-phase structures should be used. In the extension of the proposed topology to the three-phase systems without using transformer, attention should be paid that the dc voltage sources in the different phases must be independent (isolated)so that the load can be star/delta connected. It is very important to note that also in the well-known CHB topology (extended to three-phase), independent dc voltage sources are required fordifferent phases [18]. Therefore, from this point of view, the proposed topology acts as like as the CHB topology. Two conditions can be considered regarding the value of the dc voltage sources used in the proposed multilevel inverter; all of them can be equal leading to a symmetric topology or theirvalues can be different leading to asymmetric topology. These two conditions are discussed as follows.

1. Proposed Symmetric Multilevel Inverter:

For the symmetric multilevel inverter, all of the dc voltage sources are considered to be equal. Therefore, the following equations can be written for the symmetric topology:

(10)

(11)

Where Nlevel is the number of output voltage levels.

Since in the case of the symmetric topology the cascaded submultilevel inverters have the same condition, the following relations can be expressed regarding the standing voltage on the switches:

(12)

(13)

WhereVstand,total is the total standing voltage on the switchesof the multilevel inverter.Using (11), m is obtained as follows:

(14)

From (13) and (14), the following equation is obtained:

(15)

2) Proposed Asymmetric Multilevel Inverter:

For the asymmetric topology, the value of the dc voltage sources is different from a submultilevel inverter to another. In other words, if the dc sources of the first submultilevel inverter is Vdc,1, the dc sources of the second submultilevel inverter is Vdc,2 . To get maximum number of level for the output voltage, there must be no redundancy. This is achieved when the value of the dc voltage sources in submultilevel inverters have the following relation:

(16)

Therefore, in general, the following relation should be valid for the dc sources of the submultilevel inverters:

(17)

Where Vdc,iis the value of the dc sources in the i^{th} submultilevel inverter. The maximum value of the output voltage (sum of all dc voltage sources) for the proposed asymmetric topology can be obtained as follows:

(18)

Using (17) and (18), the maximum value of the output voltage can be written as

(19)

With the aforementioned arrangement of the dc voltage sources, the number of voltage levels will be equal to

(20)

For the asymmetric topology, the total standing voltage of the switches (Vstand,total) is sum of standing voltages on the switches of the submultilevel inverters ( ) and also the standing voltage on the switches of the H-bridge part (4Vo,max). Therefore, it can be written as follows

(21)

Using (5), (17), (19), and (21), the total standing voltage of the switches can be written as follows:

(22)

Using (20) and (22), the total standing voltage in terms of number of output voltage level and n can be expressed as follows:

(23)

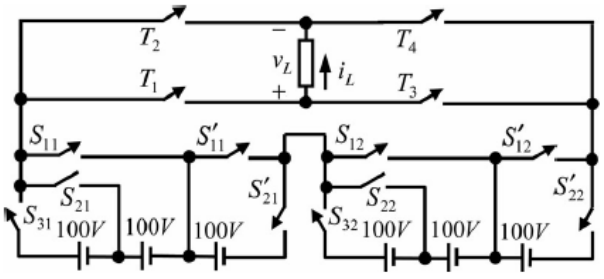

Fig. 3. The proposed symmetric topology with n = 3 and m = 2.

III.SIMULATION RESULTS

This section deals with the simulation validationof the proposed multilevel inverter topology. For the proposedsymmetric multilevel inverter, only the simulation resultsare presented, but, for the asymmetric topology the

simulationresults are given.For all of the studies, the load is an RL load with the valueof 45 Ω and 55 mH. The output voltage frequency is assumed50 Hz.There are many control methods for multilevel inverter. It isnoticeable that the staircase control method is used in this paper[1]. The term staircase control method is used to state that inthis method, transition from one level of voltage to the next levelhappens once as shown in Fig. 4 (for example). This controlmethod tends to generate a staircase voltage which minimizesthe error with respect to the reference voltage. It is worth notingthat the calculation of optimal switching angles for differentgoals, such as elimination of the selected harmonics and minimizingtotal harmonic distortion (THD), is not the objective ofthis paper.

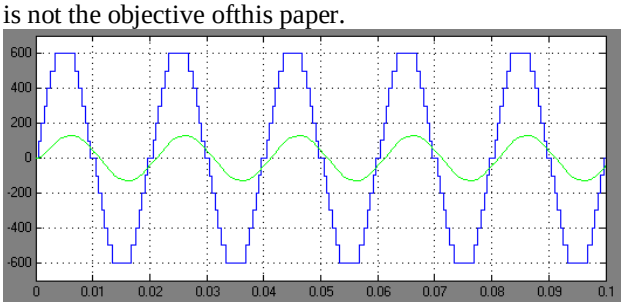

Fig. 4. Simulation results for the 13-level symmetric topology.

A. Symmetric Topology

Fig. 3shows the proposedsymmetric multilevel inverter with n=3. Six dc voltage sourceseach of them 100 V have been used so that the maximum outputvoltage will be 600 V for the 13- level inverter. The number of IGBTs for a 13-levelinverter in the proposed topology is 16. Fig. 4 shows the load voltage and scaled load current of the 13-level inverter. As well as 17- level inverter with n=4. Eight dc voltage sources are taken each of them 100V have been used so the maximum output voltage will be 800V.

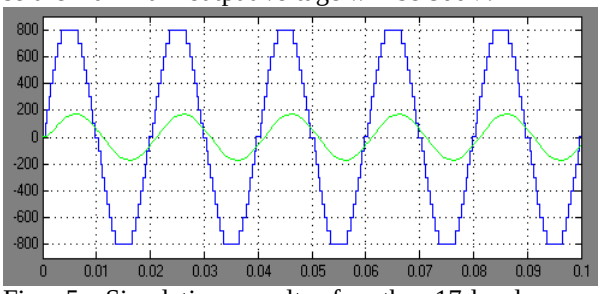

Fig. 5. Simulation results for the 17-level symmetric topology.

Fig. 5 shows the load voltage and scaled load current of the 13-level inverter. As the figure shows, all of the expectedvoltage levels are generated at the output voltage. The loadvoltage is sine-waved current as a result of theRL load whichOperates as a low-pass filter for the current. The load current has also phase difference with the load voltage because of inductive characteristic of the load.

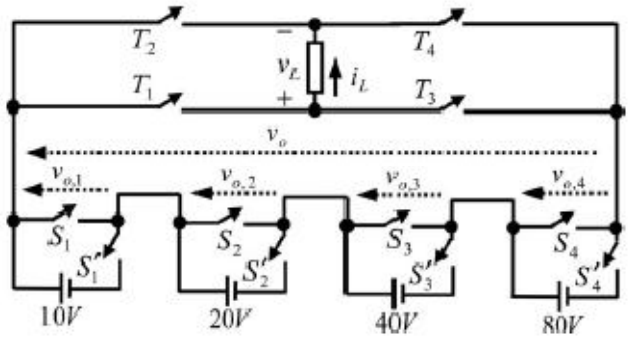

Fig.6. Thirty-one-level inverter based on the proposed optimal structurewith n = 1 and m = 4

B. Asymmetric Topology

For the asymmetric topology, first a design example of the proposed multilevel inverter is given and then it is used for simulation.

1) Design Example:

The aim is to design a peak 150-V multilevel inverter with minimum 30 levels of output voltage. As discussed before, the proposed multilevel inverter is optimal for n = 1 from different points of view. In order the number of output voltage level to be higher than its minimum (i.e., 30), the number of cascaded submultilevel inverters should be 4 (m = 4). Therefore, a 31-level 150-V inverter based on the proposed generalized multilevel inverter regarding the optimal structures will be as shown in Fig. 6 in which the values of the dc voltage sources are shown in the figure. The proposed 31-level inverter in Fig.6 uses 12 IGBTs. The number of the dc sources is 4 with binary increment. On the other hand, a 21-level inverter based on the topology presented in [13] uses 20 IGBTs which is much more than the number of IGBTs in the proposed topology, and at the same time, the number of output voltage level is lower than that of the proposed topology. A 17-level inverter based on [12] uses 16 IGBTs and 4 dc voltage sources. In comparison with the proposed topology, shown in Fig.6, the topology presented in [12] uses more IGBTs, and at the same time, the number of output voltage levels is considerably lower.

2) Simulation Results:

The validity of the proposed multilevel inverter is demonstrated with both simulation results. For the simulation, the 31-level inverter shown in Fig. 5 is used. For a switch in the inverter, an isolated driver circuit is required. The isolation is achieved using optoisolators.

Fig. 7 shows the output voltage of the cascaded submultilevelinverters, load voltage, and scaled load current. As shown in thefigure, the output voltage of the cascaded submultilevel inverters is always nonnegative. The polarity of the voltage is changed using the H-bridge connected to the output of the submultilevel inverters. The load current is scaled to become visible in the same frame with the load voltage. In the test condition (R = 45Ω, L = 55 mH, Vo,max

= 150 V), the power loss of the proposed multilevel inverter, shown in Fig. 6, is about 12W. However, the power loss of the asymmetric CHB topology with the same conditions (with the same value of voltage and load) is about 15.5 W. This can be as a result of the fact that in the proposed topology, less semiconductor devices are in the current path in any instant of time in comparison with the asymmetric CHB topology. In this condition, output active power of the inverter is about 217 W. Also, the specification of the switches (their resistance and on-state voltage) is as given in Section IV.

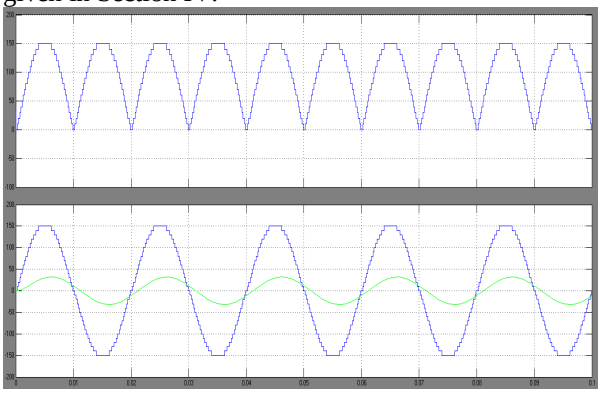

Fig. 7. (Upper trace) Output voltage of cascaded sub multilevel inverters. (Lower trace) Load voltage and scaled load current.

IV.CONCLUSION

This project proposes, initially, a sub multilevel inverter has been proposed and then the cascaded submultilevel inverters have been considered as a generalized multilevel inverter in both symmetric and asymmetric conditions. The number of the dc voltage sources in each submultilevel inverter is equal, but their values are different from one submultilevel inverter to another. Therefore, the proposed multilevel inverter can be categorized in asymmetric group. In this project 13-level and 17- level symmetric topology based on the proposed multilevel inverter have been presented. In the case of asymmetric topology, the simulations have been presented for a 31-level inverter based on the proposed optimal structure to validate the ability of the proposed topology in generating of desired output voltage.

REFERENCES

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] J. H. Kim, S. K. Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage-source inverter," IEEE Trans. Ind. Appl., vol. 44, no. 4, pp. 1239–1248, Jul./Aug. 2008.
using a novel topology," Elsevier J. Electric Power Syst.

[3] O. Lopez, J. Alvarez, J. Doval-Gandoy, F. D. Freijedo, A. Nogueiras, A. Lago, and C. M. Penalver, "Comparison of IEEE Trans. Ind. Electron., vol. 58, no. 8, pp. 2643–2650, Aug. 2010.the FPGA implementation of two multilevel space vector PWM algorithms," IEEE Trans. Ind. Electron., vol. 55, no. 4, pp. 1537–1547, Apr. 2008.

[4] A. A. Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltagesharing converter to supply single-phase asymmetrical four-level diode clamped inverter with high power factor loads," IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2507–2520, Oct. 2010.

[5] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral point clamped inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[7] M. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive application," in Proc. Appl. Power Electron. Conf., 1998, vol. 2, pp. 523–529.

[8] A. Rufer, M. Veenstra, and A. Gopakumar, "Asymmetric multilevel converter for high resolution voltage phasor generation," in Proc. Eur. Conf. Power Electron. Appl., Lausanne, Switzerland, 1999, pp. 1–10.

[9] J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," IEEE Trans. Ind. Electron., vol. 58, no. 2, pp. 412–420, Feb. 2011.

[10] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," presented at the IEEE PowerTech. Conf., vol. 3, Bologna, Italy, 2003.

[11] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, "Modular multilevel inverter: pulse width modulation and capacitor balancing technique," IET Power Electron., vol. 3, no. 5, pp. 702–715, 2010.

[12] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[13] E. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. Tarafdar Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters

Res., vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[14] E. Babaei and M. S. Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem," Elsevier J. Energy Convers. Manage., vol. 51, no. 11, pp. 2272–2278, Nov. 2010.

[15] Y. Hinago and H. Koizumi, "A single phase multilevel inverter using switched series/parallel dc voltage sources,"

[16] J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC (ANPC) converter for grid connection of large wind turbines for distributed generation," IEEE Trans. Power Electron., vol. 26, no. 3, pp. 961–972, Mar. 2010.

[17] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diodeclamped H-bridge cells," IEEE Trans. Power Electron., vol. 26, no. 1, pp. 51–64, Jan. 2011.

[18] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Ind. App., vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.

[19] E. Babaei, "Optimal topologies for cascaded sub-multilevel inverters," J. Power Electron., vol. 10, no. 3, pp. 251–261, May 2010.

[20] W. K. Choi and F. S. Kang, "H-bridge based multilevel inverter using PWM switching function," in Proc. Int. Telecomm. Energy Conf., 2009, pp. 1–5.

[21] J. F. Chen, J. N. Lin, and T. H. Ai, "The techniques of the serial and paralleled IGBTs," in Proc. IEEEInd.Electron.Soc., 1994, vol. 2, pp. 999– 1004.

[22] Y. Xiao, B.Wu, F. A. DeWinter, and Reza Sotudeh, "A dual GTO currentsource converter topology with sinusoidal inputs for high-power applications," IEEE Trans. Ind. Appl., vol. 34, no. 4, pp. 878–884, Jul./Aug. 1998.

[23] B. Abdi, A. H. Ranjbar, G. B. Gharehpetian, and J. Milimonfared, "Reliability considerations for parallel performance of semiconductor switches in high-power switching power supplies," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2133–2139, Jun. 2009.

[24] M. H. Rashid, Power Electronics: Circuits, Devices and Applications, 3rd ed. Upper Saddle River, NJ: Pearson Education, 2003.

PUTTA MAHESWARA currently pursuing his M.Tech in Power Electronics from JNTUA University, Anantapur. He had done his B.Tech degree from Moorthy Institute of Technology and Science Affiliated to JNTUH University, HYD in 2010 and his field of interest includes Power Electronics**.**

M.VIJAYA KUMAR has completed his B.Tech in Electrical & Electronics Engineering in 2007 from Sri Sai institute of technology and Science, Rayachoti, Kadapa (dt) affiliated to JNTUA University, Anantapur, M.TECH in Power Electronics in 2013 from LORDS INSTITUTE OF TECHNOLOGY AND SCIENCE, HYDERABAD, working as Assistant Professor at Sri Sai institute of technology and Science, Rayachoti, Kadapa (dt), and Andhra Pradesh, India. His area of interest includes power electronics and Drives System.

V.PRATAPA RAO has completed his B.Tech in Electrical & Electronics Engineering in 2003 from R.G.M college of engineering and technology affiliated to JNTUH University, M.TECH in Power Systems from AITS Rajampet affiliated to JNTUA University, and presently he is interested to reach topics includes power system especially in ELECTRICAL DISTRIBUTION SYSTEM, working as Assistant Professor and HOD of EEE department at SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE, Affiliated to JNTUA university, Rayachoty, Kadapa (dist), Andhra Pradesh, India.