INTERNATIONAL JOURNAL OF RESEARCH
In Advanced Engineering Technologies

Volume 2, Issue 1 SEP 2014

DESIGN AND IMPLEMENTATION OF MULTIBAND FLEXIBLE INTEGER-N DIVIDER FOR COMMUNICATION APPLICATIONS

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ABSTRACT: This project is highly useful and recommended for communication applications like Bluetooth, Zigbee. WLAN frequency synthesizers are proposed based on pulse-swallow topology and the designed is modeled using Verilog simulated using Modelsim and implemented in Xilinx. Frequency synthesizer is one of the important elements for wireless communication application. The speed of VCO and prescaler determines how fast the frequency synthesizer is. A dual modulus prescaler contains logic gates and flip-flops. To fulfill the need of high frequency and low voltage circuit suitable flipflops must be selected. Four different classes of flip-flops like master-slave, pulse-triggered, differential and dual-edge triggered (DET) are analyzed. Higher clock load in pulse-triggered FF and switching on both side of clock cycle in DET made them unusable in practical design for prescaler circuits. Due to this reason dual-edge triggered and pulse-triggered flip-flops are not taken for the comparison. Divide-by-2/3 prescaler is implemented by TSPC, ETSPC master-slave and differential type of flip-flops.Different 32/33 prescalers are implemented by choosing various combinations of 2/3 prescaler and flip-flops. Prescalers using different FFs are compared in terms of operating frequency, power, delay and power-delay-product

Keywords—Clock distribution networks, clock trees, clock skew,clock skew scheduling, CMOS, H-trees, interconnect delay, process variations, RLC impedances, synchronization, timing optimization.

I. INTRODUCTION

In a synchronous digital system, the clock signal is used to define a time reference for the movement of data within that system. Since this function is vital to the operation of a synchronous system, much attention has been given to the characteristics of these clock signals and the networks used in their distribution. Clock signals are often regarded as simple control signals; however, these signals have some very special characteristics and attributes. Clock signals are typically loaded with the greatest fan-out, travel over the longest distances, and operate at the highest speeds of any signal, either control or data, within the entire system. Since the data signals are provided with a temporal reference by the clock signals, the clock waveforms must be particularly clean and sharp. Furthermore, these clock signals are particularly affected by technology scaling, in that long global interconnect lines become much more highly resistive as line dimensions are decreased. This increased line resistance is one of the primary reasons for the growing importance of clock distribution on synchronous performance. Finally, the control of any differences in the delay of the clock signals can severely limit the maximum performance of the entire system as well as create catastrophic race conditions in which an incorrect data signal may latch within a register.

Wireless LAN (WLAN) in the multigigahertz bands such as Hiper LAN IT and IEEE 802.11 a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like

IEEE802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL) , is one of the power-hungry blocks in the RF front-end and the first stage frequency divider consumes a large portion of power in frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz consume up to 25mW in CMOS realizations, where the first stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range.

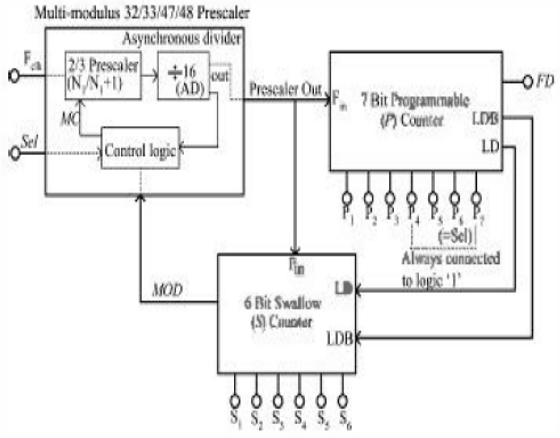

Fig.l.Proposed dynamic logic multiband flexible Divider.

In this paper, a Dynamic logic multiband flexible integer-n divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler as shown in Fig.l The divider also uses an improved low power loadable bit-cell for the Swallow S-counter. a true single-phase-clock (TSPC) policy was introduced. Single-phase-clock policies are superior to the others due to the simplification of the clock distribution on the chip and reducing the transistor number. They reduce the number of clock-signal requirements and the wiring costs also they have no problems with phase overlapping. Thus, higher frequencies and simpler designs can be achieved. Further enhancement in the design is achieved by using extended true-single phase clock (ETSPC) DFFs.

Clock Generation

There are many issues to consider in the design of a clock generator. Both power dissipation and jitter play a major role in determining the type of generation system to utilize. Obviously, operating frequency also plays a major role, especially in the present day systems. The large discrepancy between system clock frequency and processor clock frequency inevitably results in the need for a phase locked loop (PLL) clock generator.Figure: a illustrates the basic block diagram of a phase locked loop (PLL)-based clock generator. The benefits of such a clock generator are two-fold. First, the frequency of the clock generator output can be a multiple of the main system clock frequency. This allows the integrated circuit to run at a higher frequency than the rest of the system, while maintaining synchronization. This is important for microprocessors, because the advancement of the system bus frequency has traditionally lagged the advancement of the microprocessor frequency. Use of an on-chip PLL has allowed microprocessors to continually increase in performance while only marginal gains in system bus performance were made. Second, in a synchronous system, use of a PLL clock generator can eliminate clock skew from active device variation between chips or even on the same chip. Since the output of the PLL is in-phase with the input, if the clock distribution bu ers are included within the loop (as illustrated in Figure: a), their delay is essentially removed from the system.

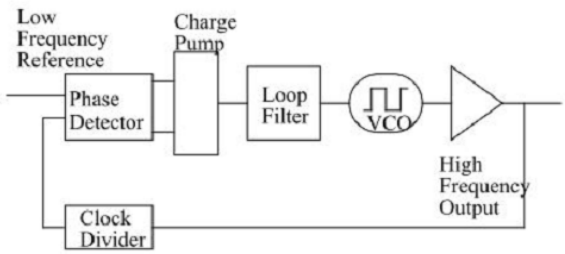

Figure :a : A generic phase locked loop (PLL) block diagram.

II. Conventional TSPC Based Div-By-2/3 Prescaler

The TSPC architecture has the advantage of a higher operating frequency compared to that of master-slave and differential flip-flops. In order to reduce the power consumption and propagation delay digital gates are embedded into the flip-flops where the conventional 2/3 prescaler consists of an OR gate, AND gate and two D flip-flops [5]. The conventional 2/3 prescaler uses two DFFs where DFF1 is loaded by an OR gate and DFF2 is loaded by DFF1, an AND gate and an output stage which makes a larger load. This large load on DFF2 causes substantial power dissipation and limits the speed of operation. The difficulty in embedding the OR, AND gates into the DFF introduces additional delay by the digital gates which limits the speed of operation in conventional one. A low power and improved speed 2/3 prescaler implemented in the TSPC logic format is proposed in [13]. Fig 4 shows the new prescaler which uses two neither embedded NOR gates instead of an OR and an AND gate for the conventional 2/3 TSPC prescaler. This arrangement reduces the number of switching nodes from 12 to 7 and consumes less power compared to the conventional 2/3 prescaler.

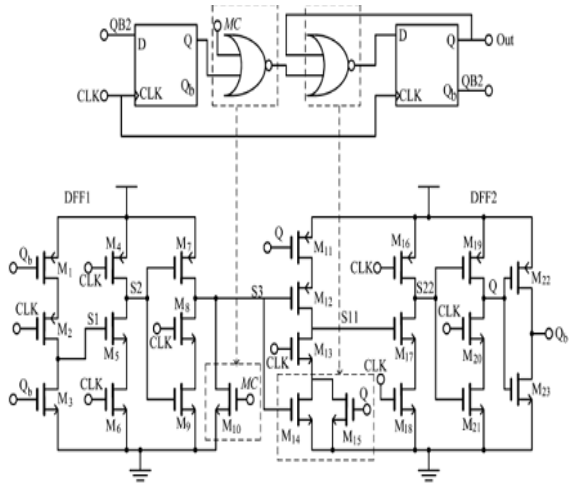

Fig 4: Design-I TSPC 2/3 prescaler circuit and equivalent gate level schematic.

Later an ultra-low power 2/3 prescaler (Design-II) in [13], a further improved version of the Design-I is shown in Fig 5. In this design a pMOS transistor, connected between power supply and DFF1 with the control logic signal MC selects the divide-by-2 or divide-by-3 mode. When MC is logically high DFF1 will disconnected from the power supply and DFF2 alone work to form the divide-by-2 operation. Therefore the short circuit power and switching power of DFF1 is removed. When the control signal MC goes low pMOS transistor will turns on and both flip -flops combine give the divide-by-3 operation. Operating frequency is directly related to the supply voltage. Since due to the Vds drop across transistor M1a, DFF1 operates at a decreased voltage level which limits the maximum operating frequency [13]. However, by decreasing the stacked connection in the first stage of Design-II similar to the design in [10] improves the frequency range to almost same as that of the Design-I.

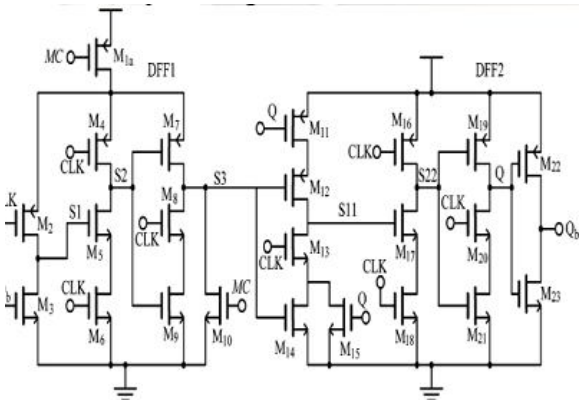

Fig 5: Design-II TSPC 2/3 prescaler

III. ETSPC 2/3 PRESCALERS

As a part of increasing operating frequency and reducing supply voltage ETSPC FFs outstand the TSPC FFs. The two major conventional divideby-2/3 ETSPC designs are in [10] and [11]. Design in [10] causes redundant power consumption in the div-by-2 mode operation. Design in [11] overcomes the toggling of FF1 during divide-by-2 operation by
Changing the control logic from output of FF1 to its input. But the first stage in design [11] causes larger power consumption. Eventhough both designs are simpler, the inverter between both flip-flops and parallel connected transistor introduce extra delay and larger parasitic capacitance [7]. To prevent these issues a new method is proposed using ETSPC

technique.

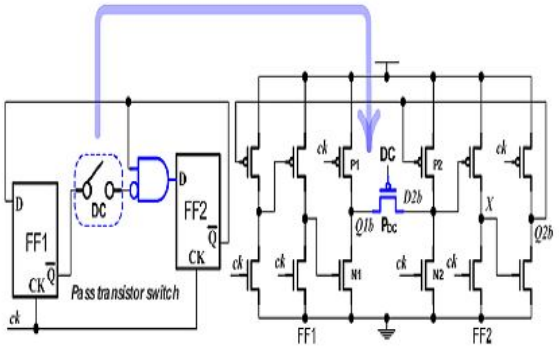

Fig 6: Schematic of proposed E-TSPC based divideby-2/3 prescaler

Fig 6 shows the schematic of proposed ETSPC design. The structure shows that output Qbar of FF1 is complemented and given to one of the AND gate's input. The pMOS transistor with input DC acts as a control switch, selects the mode of operation. The proposed method has the advantage of reduced propagation delay by avoiding the inverter implementation between two flip-flops and integrating the logic gates without any extra transistors. When control signal DC is logically high, the FF1 will disconnect from FF2 and it alone does the divide-by-2 operation.

IV. DIV-BY-32/33 PRESCALERS

Fig 7 shows the topology of a general 32/33 prescaler. The circuit contains one 2/3 prescaler unit, combination of NAND and NOR gates and four stages of toggled divide-by-2 units using DFFs. When the control signal MC is logically high, the 32/33 prescaler function as divide-by-32 unit and the control logic signal MC to the 2/3 prescaler goes logically high allowing it to operate in divide-by-2 mode for the whole 32 clock cycles. When control logic signal MOD is logically low, the 32/33 prescaler unit function as divide-by-33 unit during which 2/3 prescaler operates in divide-by-3 mode for 3 input clock cycles and in divide-by-2 mode for 30 input clock cycles [13].

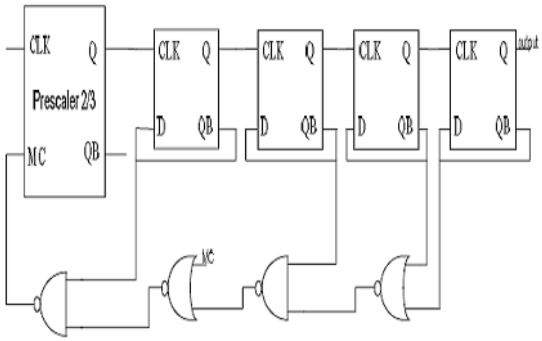

Fig 7: Logic structure of divide-by-32/33 counters design.

V. EXPERIMENTAL RESULTS

A comparison and complete analysis of the performance of various prescalers is carried out using Cadence virtuoso for 180nm CMOS process. TABLE 1 shows the simulation results of the operating frequency and power consumption of dual-modulus prescaler using different flip-flops for the operations of divide-by-2 and divide-by-3. The simulations are done at a supply voltage of 1.8V. Flip-flops, which are selected for prescaler designs come under different classifications such as master slave, differential, TSPC and ETSPC technique.

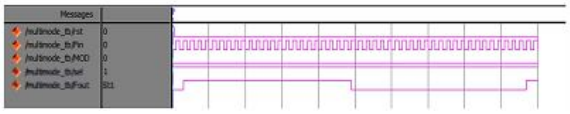

Fig.8.Divide-By-32

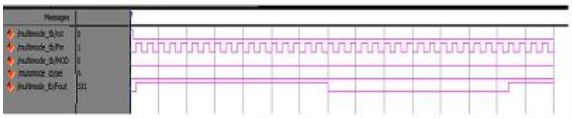

Fig.9.Divide-By-33

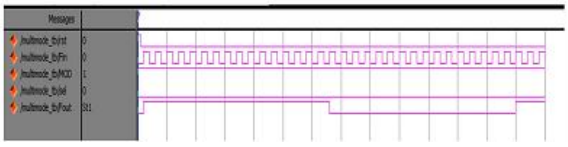

Fig.10.Divide-By-47

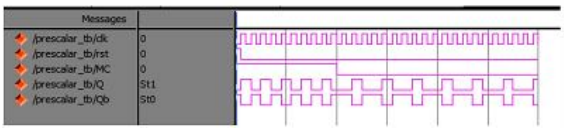

Fig.11. Prescaler 2/3

Table 1: Feature Comparison Of Various Divide-By-2/3 Counter Designs Under 180nm Technology.

Flip-Flop	V_{DD} (V)	Operating frequency	Div-by-2 P(mW)	Div-by-3 P(mW)
WPMS	1.8	300 MHz	0.8	1.27
MSAFF	1.8	335 MHz	1.16	1.26
STFF	1.8	351 MHz	0.58	1.372
Design-II using TSPC	1.8	3.25 GHz	1.159	1.665
Proposed design using ETSPC	1.8	5 GHz	1.663	2.217

On-wafer measurements are carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the 8600A 6G oscilloscope.

The measurement results shows that the wideband 2/3 prescaler has a maximum operating frequency of 6.5 GHz [10] and the multi modulus 32/33/47/48 prescaler designed using wideband 2/3 prescaler has a maximum operating frequency of 6.2 GHz. However, the maximum operating frequency that can be achieved by the multi modulus 32/33/47/48 prescaler is limited by the wideband 2/3 prescaler.

The performance of the multiband flexible divider is measured in both the lower frequency and higher frequency bands by programming the P-and Scounters. Fig. 8 shows the measured output waveform of the multiband divider at an input frequency of 2.47 GHz where counters are programmed to have values 77 and 6 respectively.

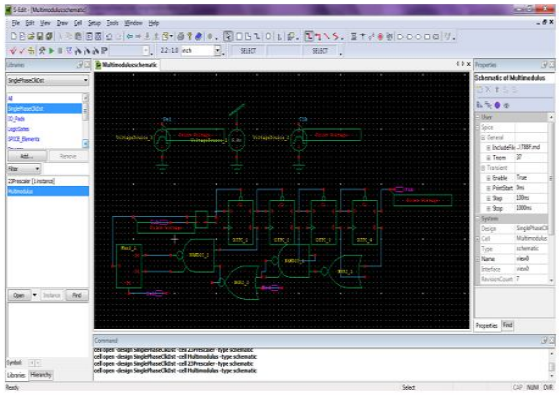

Fig 12: Designing of Multimodulus

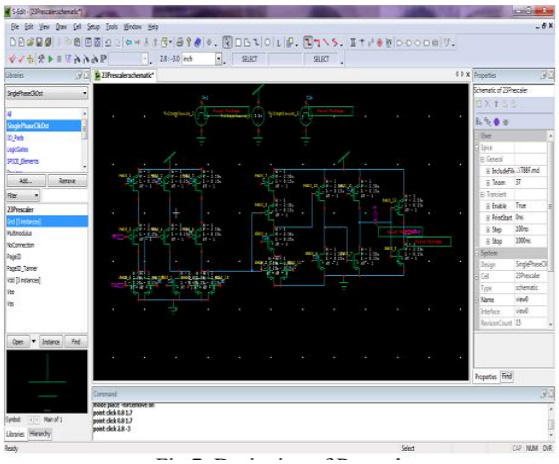

Fig 13: Designing of Prescaler

VI. CONCLUSION

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multi modulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler, and is silicon verified using the 0.18micro meter CMOS technology. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. However, since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P and S-counters are programmed accordingly. The

proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow _-counter and consumes a power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing. By using this multimodulus prescaler, the Clock Jitter can be avoided.

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