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VLSI IMPLEMENTATION OF SINGLE CYCLE ACCESS STRUCTURE FOR LOGIC TEST IN FPGA TECHNOLOGY

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ABSTRACT:

In this paper single cycle access test structure for logic test eliminates the power consumption problem of conventional shift based scan chains and reduces the activity during shift and capture cycles. But it had more complicated in instruction like floating point and it need maximum area. So we propose a priority encoder in the single cycle access test structure to speed up the execution process and reduce the peak power consumption problems. This paper proposes a new single cycle access test structure for logic test. This leads to more realistic circuit behavior during stuck-at and at-speed tests .So here we are developing paper by using HDL language, simulated modelsim6.4b and synthesized Xilinx ISE10.1.

Key Words: Low-power testing, Test power reduction, Test-time reduction, Test area reduction, single cycle access, priority encoder.

1. INTRODUCTION

The production test costs of chips become more and more dominant. The standard shift scan (SS) method is the most popular test implementation within the last decades. It has been tried to improve this approach in terms of test time, test data volume and test power by optimizing the scan pattern, using different scan chain structures, different scan support logic, or a combination of these modifications. Automatic test pattern generation (ATPG) for sequential VLSI circuits is an NP-complete problem with an exponential complexity. The complexity of combinatorial logic varies. Less complex logic is tested within a few capture cycles, generating an immense number of don't cares during the rest of the test, even when test compression methods are used. Complex and hard to test logic needs to be stimulated and captured quite often but the pattern need to be shifted throughout the complete scan chain. One approach to reduce test time is to use parallel scan chain. This leads to a massive increase of parallel scan chains to reduce the length of the scan chains. In order to further reduce test data volume, a built-in-self-test (BIST) mechanism is used.

II. SCA-STRUCTURE WITH HOLD MODE

A. SCAh-FF

The key element of the single cycle access structure with hold mode (SCAhS) is the signal cycle access register (Flip-Flop, FF) with hold mode (SCAh-FF). It is based on a standard scan register (S-FF) and uses two more 2-to-1 multiplexers. The SCAh-FF has one more input and one more output compared to the standard shift register (S-FF). The inputs clock {clk}, data-in {di}, and scan-in {si} still exists. The scan-enable is now a 2 bit bus {se[0:1]}. An additional scan output pin {so} is added. The reset input and inverse output pins are not shown. The internal logic enables the register to run in one additional hold mode, whereas the additional output multiplexer can bypass the register to directly drive the value of {si}. The resulting functionality

is best explained by a truth table.

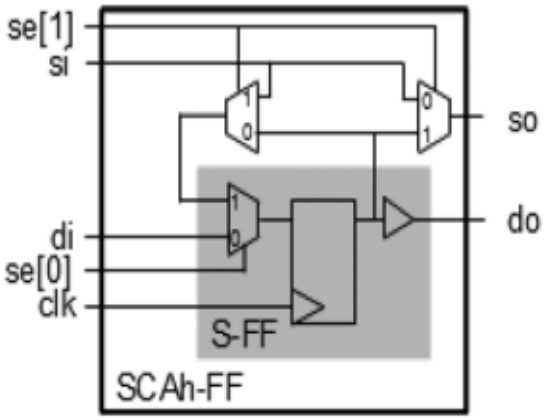

Fig 1: SCAh-FF based on an S-FF

TRUTHTABLE OF SCAh-FF

se[0:1]	do @ clk	so	mode
00	di	si	functional
01	di	do	async. read
10	do, unchanged	si	hold
11	Si	do	sync. write/read

The slave latch of a FF is usually connected to the output driver of the data-out pin and/or an inverting driver for the inverse-data-out pin. The internal multiplexer for the SCAh-FF can also be driven by this slave latch output. The fan-out number of the data-out pin (or inverse-data-out pin) refers to the number of input pins which are driven by the SCAh-FF data output drivers.

In functional mode ({se[0:1]}=="00"), the register captures {di} and { so} follows { si} (usually stable). In read mode {so } has the value of {do } so that {do } can be read out asynchronously. In the event of the relevant clock edge, the register captures {di}. In hold mode, {so} follows {si}, and the register remains in the state {do}, capturing its own value. When {se[0:1]}=="11", the registers captures {si} and {so} changes to the new value of {do} (sync. write/read mode)

B. SCAh-FF Connectivity

The SCAh-FF and its connectivity. The two major differences are, that the scan-in {si} is now connected to a dedicated scan-out {so } of the preceding register in the scan chain and the register {se[1]} inputs on the same scan depth are connected to the same line-select {Is} signal, which is driven by a "1 out of N" decoder. SCAh-FF connected to the same line-select signal are considered to be on one line. If {add} is 0, no line is selected. {se[0]} of each SCAh-FF is connected to the global scan enable signal {gse} (comparable to the global scan enable signal of shift-scan structures). The output of the address decoder is connected to the {se[1]} pin of the registers on one particular line. Instead of shifting the data through the scan chain, all registers on the same scan depth, enabled by the same line-select signal can be read or written with a single cycle access. Additionally, unselected registers remain in hold mode. From this structure four different kinds of cycle modes result.

1) When {gse} is low and {add} is 0, the design works in normal functional mode.

2) If a specific address is given (asynchronous read), the register values on the selected line are passed to the scan-out bus {so}. This mode is

called asynchronous read mode.

3) When {gse} is high and {add} is 0 (no line selected), the design remains in hold mode and no register value changes during an clock edge.

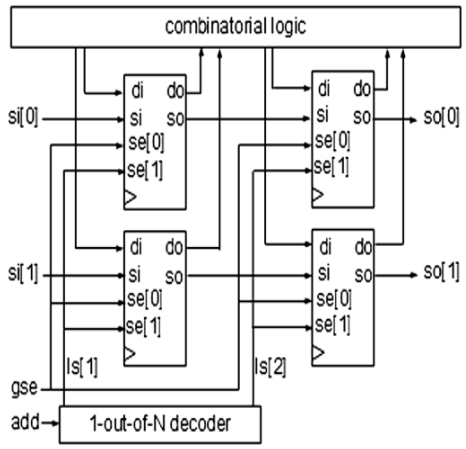

Fig 2: SCAhS connectivity

4) If a specific address is given at a relevant clock edge and {gse} is high, the scan-in values {si} are captured by the registers on the selected line (synchronous write) and scan-out {so} is driven by the captured register value (read). This mode is called synchronous write/read. The structure is backward compatible to known shift scan operations if {add} is set to 1 at the beginning and automatically incremented after each "shift" cycle. The shift-in data can be written continuously throughout the scan area and the scan-out data can be read at the same time. A capture cycle can also be applied to all registers at the same clock edge (functional mode).The setup time of the SCAh-FF equals the one of the S-FF, because no additional logic is added to the relevant timing path through {di}. The fan-out of {do} is reduced by one because {do} does not drive the {si} of the succeeding register, which is usually the case in SS. The new scan-out {so} drives the {si}of the succeeding register in the scan chain and has a constant fan-out of 1. The scan chain is decoupled from the functional logic.

C. SCAh-FF Page Organization

The SCAhS enables single cycle read/write accesses to the individual register line. The test structure is now organized in pages to achieve a read/write access at design speed or at a reasonable test speed. The page depth equals the scan chain depth (SD = number of SCAh-FF connected to one chain on one page). Assuming it is 31. Multiplied with the scan width (SW = number of scan chains on one page, for instance 32), the resulting number of SCAh-FF is 992 per page.

In this rather extreme compact case, the page uses a global 1-out-of-31 address line decoder. A page selector {pse} selects the individual page and drives the scan input bus signals and line select { Is} signals (AND-ed) only of this particular page.{pse} can be driven by a register which is set by a dedicated test control logic. If not selected, the page remains inactive to reduce activity. The scan output buses of all pages {so} are bit-wise XOR-ed with the {so} of other pages to generate the global scan-out bus {pso}. If the page is inactive, the XOR-tree passes the value of previous pages unchanged since all {so} bits of an unselected page are "0". With the page organization, the relevant timing paths become clear. During a read, the registers are selected by the line-select signal and drive the scan-out bus {so} through a multiplexer chain of the succeeding registers and the page-scan-out bus {pso} through the XOR-tree. During a write, the scan-in bus {si} values are passed through the AND-selector and the multiplexer chain of the trailing register to the registers of the selected line.

In order to achieve a high test speed, the test implementation can be pipelined. The scan-in bus {si} and the line-select {Is} outputs of the global address-decoder can be registered. Also the XOR-tree can be pipelined with buried register sets. For eight pages a logic depth of three XOR-cells can be reached. If an optimal test speed cannot be achieved, the scan-depth SD can be reduced (to any number). It is important to notice, that there is no timing path between adjacent registers on the scan chain during test mode ({so}->{si}). Therefore, no hold time problems exists,

which are known from shift-scan-test, and no buffers must be inserted for hold time fixes.

D.AREA

The areas of various cores with the standard scan implementation and the areas of the cores with the proposed structure are compared using the ISE10.1 library. The cores are processors (CPU, OR1200), a DMA-core and peripherals (AES, ETHER, PCI).For the calculation of the standard shift (SS) area, each register (FF) is replaced with the corresponding scan FF (S-FF). A FF with an area of nine logic units (lu) is replace with a S-FF of 11 logic units as defined in the lsi10k library. The two additional pins and the 2-to-1 multiplexer result in an area difference of two logic units. The resulting core area includes a buffered scan-enable tree and a simple XOR-tree for scan-out decompression and is listed in "A_{SS}" of Table III. Buffers for hold time fixes of the scan chain are not considered. The page support area of an SCAh-FF based implementation for each core is listed in "$A_{support}$" of Table III. This includes the XOR-tree and the two AND-selectors for scan-in and line-select. Additionally one buffer per six registers is added for each line-select signal. The area for an SCAh-FF is set to 14 logic units. Compared to an S-FF it has two more pins and two more 2-to-1 MUX, which results in an area difference of three logic units. The calculations consider the buffered scan-enable tree for SCAhS and SS. As can be seen in Table III, the resulting area "Ascah" generates an area overhead of 33.78% compared to non-test area ("A scah/A non stop") and 17.27% compared to the SS area ("A scah/ A ss") of the core logic. It does not consider memories, MBIST-logic, power-wells, spare-cells and pad logic. The number of cell pins per logic unit decreases from 1.25 to 1.18, indicating less congestion than in an SS-based design. An average of 1375 registers generates an average SCAhS area of 33.150 lu. It is assumed, that a page with 992 registers has an estimated average area of 23.916 lu. Adding a standard register (9 lu) to a page increases the area by 0.037%.

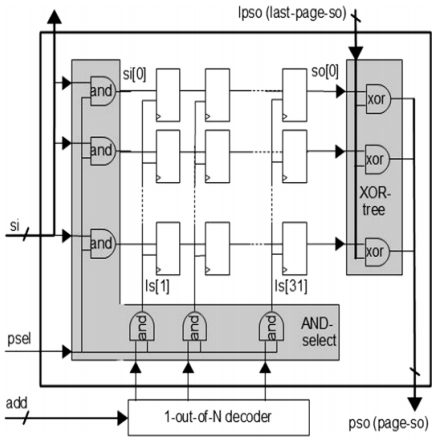

Fig 3: SCAh-page, global scan enable not shown

III.SCA -STRUCTURE WITHOUT HOLD MODE

In a tester environment, the CUT can be stimulated with controlled clock signals. Most tests can be repeated cycle accurate.To view internal register values of a S-FF-based test insertion in normal operation (at-speed), the test is stopped after a defined number of clock cycles and the register values are shifted out (one test per cycle). This procedure is repeated by adding one cycle at a time.

The SCAhS supports this procedure. With the SCAhS one particular line can be selected and continuously read out (one test per line). SW register values can directly be streamed out during one test. In other words, the SCAhS gives the same debug visibility as the shift structure, but allows the user to concentrate on selected signals when debugging extensive tests without stopping the test run.

TRUTHTABLE OF SCA-FF

se	do @ clk	so	mode
0	di	si	functional
1	si	do	sync. write, async. read

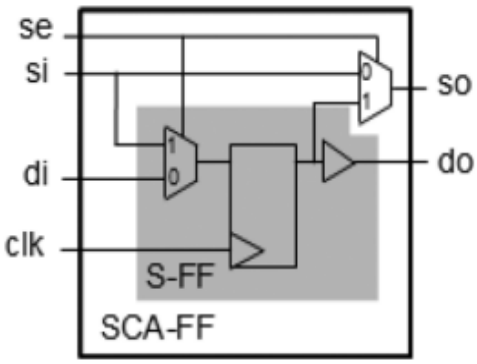

Fig 4: SCA-FF based on an S-FF

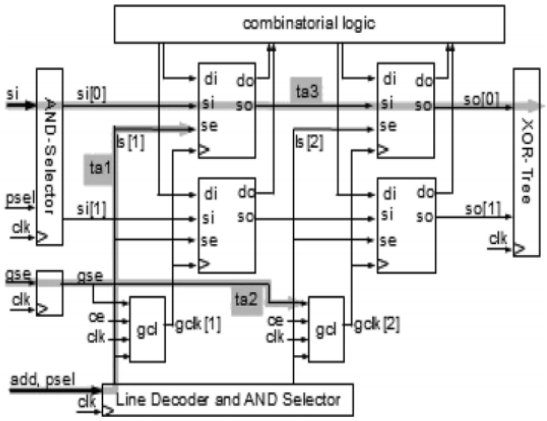

Fig 5: gSCAS connectivity

IV.SIMULATION RESULT:

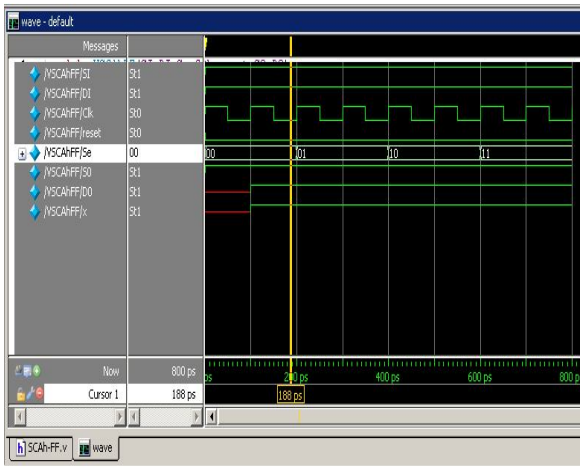

Fig 6 SCAh-FF based on an S-FF

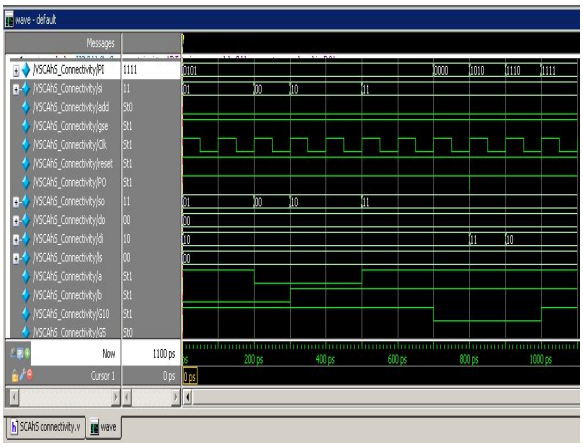

Fig 7: SCAhS connectivity

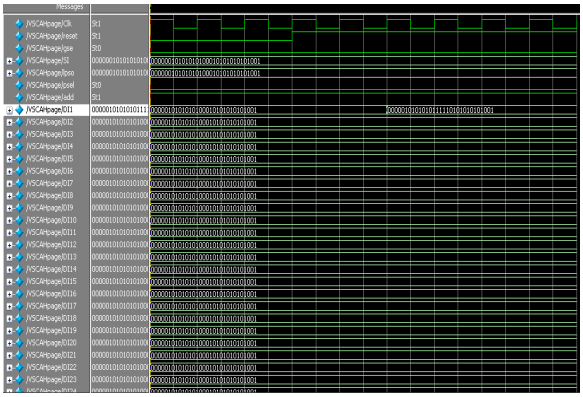

Fig 8: SCAh-page, global scan enable not shown

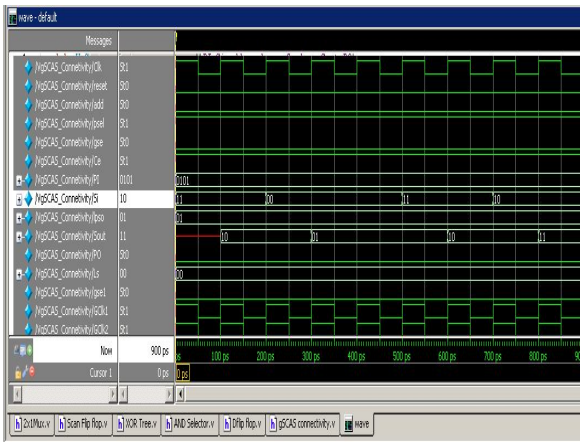

Fig 9: gSCAS connectivity

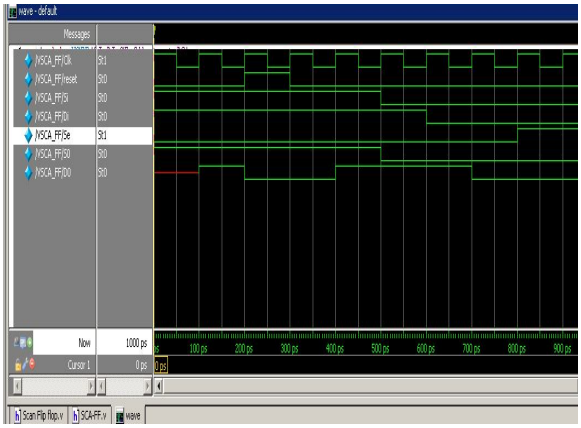

Fig 10: SCA-FF based on an S-FF

V.CONCLUSION

A single cycle access structure is discussed. Various implementations with and without hold mode as well as gated and partial implementation methods are presented. The aspects feasibility, peak power consumption, switching activity during test, area, test cycles, at-speed testing and debugging features are compared. A guide is given how to select the best implementation. The best solution (gSCAS) is compared to RAS implementations and is superior to all known RAS solutions. If BIST is preferable due to limited chip IOs or partial scan implementation, an address controlled BIST is discussed.

The ATPG algorithms can be enhanced with the same methods SS implementations are optimized. Future work is related to algorithms for reducing the test cycles per net itself, register reordering, pattern optimization for activity reduction and de-/compression methods for BIST using the gSCAS.

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