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VLSI design of a novel test for FIFO buffers permanent fault of NoC router

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Abstract: **This brief presents the concept, on-line transparent test technique for detection of hard faults during the field operation of NoC that are developed in FIFO buffers of routers. The Network-on-Chip (NoC) communication is packet based network and communicate by sending and receiving packets. Proposed transparent SOA-MATS++ test on a mesh-type The repeating test process in the technique prevents accumulation of faults. The realization of the NoC results after adding test circuit has been investigated in terms of throughput while the area overhead has been studied by synthesizing the test hardware. Synthesis and Simulation of the design is done by using Xilinx ISE Design suite.**

Key words: FIFO buffers, in-field test, NoC, permanent fault, transparent test.

I. INTRODUCTION

Over the last decade, network-on-chip (NoC) has been in demand due to its better communication infrastructure when contrasted with bus-based communication network for complex chip designs overcoming the challenges identified with bandwidth, signal integrity, and power dissipation. However, similar to all the other systems-on-a-chip (SoCs), NoC-based SoCs must also be tested for defects. Testing the components in the NoC infrastructure involves testing routers and inter router links. On the basis of the probabilities, run-time faults or defects occurring in buffers and logic are significantly higher compared with the other components of the NoC. Thus, test process for the NoC infrastructure must be started with the test of buffers and routing logic of the routers. Also, the test must be performed periodically to guarantee that no fault gets accumulated. The occasional run-time functional faults have been one of the major concerns during testing of deeply scaled CMOS-based memories.

The faults are resulted due to physical effects, such as environmental susceptibility, aging, and low supply voltage and hence are intermittent (nonpermanent indicating device damage or malfunction) in nature. However, these intermittent faults tend to become permanent when the faults are at a relatively high occurrence rate. Moreover, wear-outs of the memories also cause these faults to become frequent enough to be classified as permanent faults. Due to this, the need for online test technique that can identify the run-time faults, which are intermittent in nature but gradually become permanent over time has become more important.

Chip integration has reached a phase where an entire system can be placed in a single chip. When we say complete system, we mean all the required elements that make up a specific sort of application on a single silicon substrate. This integration has been made conceivable because of the rapid improvements in the field of VLSI designs. This is primarily utilized as a part of embedded systems. Thus, in simple terms a SoC can be characterized as "an IC, designed by combining together numerous stand-alone VLSI designs to provide complete process for an application."

NoC is viewed as a store of computational, storage and I/O resources on-chip that are linked with each other through a network of routers or switches instead of being linked with point to point wires. These resources communicate with each other using data packets that are routed through the network in an indistinguishable way as is done in conventional networks. It is obvious from the definition that we have to utilize highly sophisticated and researched techniques from traditional computer networks and implement them on chip. We have to explore the provoked factors that

are fascinating the researchers and designers to move toward the endorsement of NoC architectures for future SoCs.

Most of the area of present NoC data transport medium is occupied by First In First Out (FIFO) buffers. Accordingly, the probabilities of faults or defects occurring in buffers are significantly higher compared to the other components of the NoC. In this work, an on-line transparent test technique has been proposed for detection of run-time faults developed in FIFO buffers present within the routers of the NoC infrastructure. The test performs active fault detection over the entire FIFO buffer. In this project, the FIFO buffers are tested using a Transparent March algorithm instead of traditional March test algorithms to assure that the memory contents are not lost during test. The Transparent March test is a test that is repeated periodically to avoid formation of faults in the FIFO buffers. The data traffic moving in and out of the FIFO buffers during normal operation of the NoC is used as data background during test. Thus no data background needs to be loaded in the FIFO buffers prior to testing. An implementation of the test circuit performing the Transparent March test on the FIFO buffers is proposed. The test circuit is integrated into the router-channel interface and the on-line test is performed with different data traffic of different applications. The performance of the NoC after addition of the test circuit is investigated in terms of throughput and latency using a System C based simulator.

II. LITERATURE REVIEW

Fault tolerance in NoC design has increased its importance among research community, a number of papers have been published covering different aspects of fault tolerance, such as failure mechanisms, fault modeling, diagnosis, and so on. A detailed survey summarizing the research work in these papers has been provided. Since years, researchers have proposed numerous Design For-Testability (DFT) techniques for NoC framework testing (testing routers as well as NoC interconnect) and for NoC based core testing. Techniques used in testing are Built-in self test (BIST) and testing for routers using NoC interconnect. Recent novel on NoC and router testing provides a brief summary of the DFT techniques engaged for testing NoC interconnects and routers in particular. FIFO buffers in NoC framework are large in number and spread all over the chip. Subsequently, probability of faults is significantly higher for the buffers when compared with other components present in the router. Test techniques proposed for test of FIFO buffers in NoC include both online and offline techniques. An offline test technique (suitable for the detection of fault in FIFO buffers) that proposes a shared BIST controller for FIFO buffers. The proposed technique can be in online test for detecting faults in FIFO buffers of NoC routers. However, it employs standard cell-based FIFO buffers, while in this project we consider SRAM-based FIFO designs. Thus, faults considered in this brief are different from those targeted.

The on-line transparent test technique for detection of latent hard faults which develop in first input first output buffers of routers during field operation of NoC and also propose fault tolerant solution by introducing shared buffer in router. It provides alternative way in case of detection of faults otherwise used to improve efficiency. The technique involves repeating tests periodically to prevent accumulation of faults. NoC approach has emerged as a promising solution for on-chip communications. This proposes an on-line transparent test technique for detecting hard faults that develop in first input first output buffers of routers. The technique involves repeating tests periodically to prevent accumulation of faults. Implementation of the proposed test algorithm has been unified into the router -channel interface and on-line test has been for the given input data.

III. FAULTS IN A NOC

A NoC is an on-chip communication network that actualizes multi-hop and predominantly packet-switched communication. Through pipelined packet transmission, NoCs permit a more efficient utilization of communication resources than traditional on-chip buses. It is found that formal NoCs reduce layout complexity of VLSI when compared to conventional system.

In future chip generations, faults occur with the increasing probability, due to the susceptibility of shrinking feature sizes to process variability, age-related degradation, crosstalk, and single event upsets. To support chip production yield and dependable task, very large numbers of faults must be endured. Future technologies suggest that component failure rates may increase about 0.1. On the off chance that PCs are to profit by future advances in

innovation at that point there lie significant difficulties ahead, including how to build reliable systems on increasingly unreliable technology and how to exploit parallelism increasingly effectively, not only to improve throughput, but also to mask the consequences of component failure. Rapid development in silicon technology is enabling the chips to accommodate billions of transistors. It has been observed however, that the current on-chip interconnects buses are becoming a bottleneck as they are unable to cope with growing number of participating cores on a chip. Shrinking silicon die size will lead to enhanced levels of cross talks, high field effects and critical leakage currents which, in turn, will lead to more temporary and permanent errors on chip. Crash or permanent failures can occur due to electro migration of a conductor or a connection failure permanently halting the operation of some modules. On the other hand, faults like Gaussian noise on a channel and alpha particles strikes on memory and logic can cause one or more bits to be in error but do not cause permanent failures.

1) Firstly, transient faults can corrupt individual packets causing them to be mis-routed or invalid, in which case a retransmission is required.
2) Secondly, routers become permanently unavailable causing them to stop functioning due to electro movement, cracks, or dielectric breakdowns.

The area of NoC is still in its earliest stages, which is one reason why there are various names for the similar thing; namely on-chip networks, networks on silicon, but the most common name used is “Networks on Chips” (NoCs). As of now in this project we use, these terminologies interchangeably.NOC is integrating various processors and on chip memories into a single chip. Faults occur in NOC.

- Permanent faults
- Transient fault

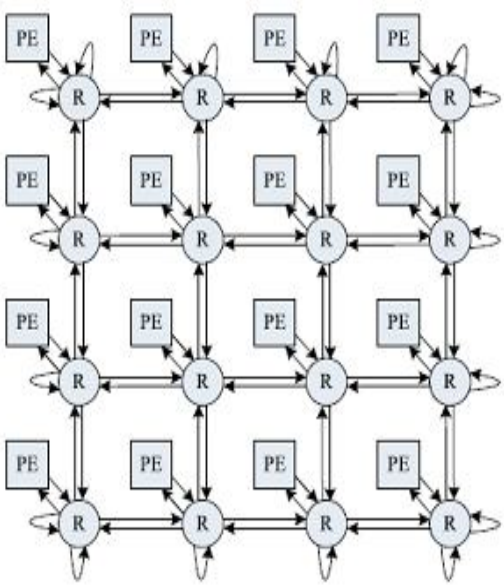


Fig 1 NoC Architecture

IV. Transparent Test Generation

The faults considered in this brief, if applied for SRAMs or DRAMs, can be detected using standard March tests. But, March test cannot be used directly due to the address restriction in SRAM-type FIFOs mentioned, if the same set of faults are considered for SRAM -type FIFOs. And thus it lead to choose the proposed single-order address MATS++ test (SOA-MATS++) for the detection of faults. SOA-MATS++ test is represented as {_ (wa); ↑ (ra,wb); ↓ (rb,wa)}; _ (ra)} where, ↑ and ↓ are increasing and decreasing addressing order of memory, a is the data background and b is the complement of the data background, _ means memory addressing can be increasing or decreasing. SOA-MATS++ test applied to the FIFO involves writing patterns and reading them back into the FIFO memory. As a result, the memory contents are destroyed. Yet, online memory test techniques require the restoration of the memory contents after test. To overcome this problem analyst altered the March tests to transparent march test that can be performed without any external data background and the memory contents can be restored after test. Finally SOA-MATS++ test is transformed to transparent SOA MATS++ (TSOAMATS++) test that can be applied for online test of FIFO buffers. The representation of transparent SOA -MATS++ test generated is as shown
{↑ (rx,w¯ x, r ¯ x,wx, rx)}.

The SOA-MATS++ test algorithm is subjected for test of different faults occurring in NoC. These faults are developed during field operation of FIFO memories they are stuck-at fault, transient fault, and read stuck-at fault, transition fault, and read disturb faults. The fault coverage of the algorithm is shown in Fig. 2. In both the figures, the word size of FIFO memory is assumed to be of 4 bits. As shown in Fig. 2, assume the data word present in lut be 1010. The test cycles begin with the invert phase (memory address pointer j with 0 value) during which the content of location addressed is read into temp and then backed up in the original. The data is driven back to SOA-MATS++ test. Lut(location under test) is the complement of content of temp. Thus, at the end of the cycle, the data present in temp and original is 1010, while lut contains 0101. Assume a stuck-at-1 fault at the most significant bit (MSB) position of the word stored in lut. Hence, it stores 1101 instead of storing 0101 and as a result, the stuck-at-fault at the MSB gets excited. In the second iteration of j, when lut is readdressed, the data read into temp is 1101. At this point, the data present in temp and original are compared (bitwise XOR ed). An all 1's pattern is expected as result. Any 0 within the pattern would mean a stuck-at fault at that bit position.

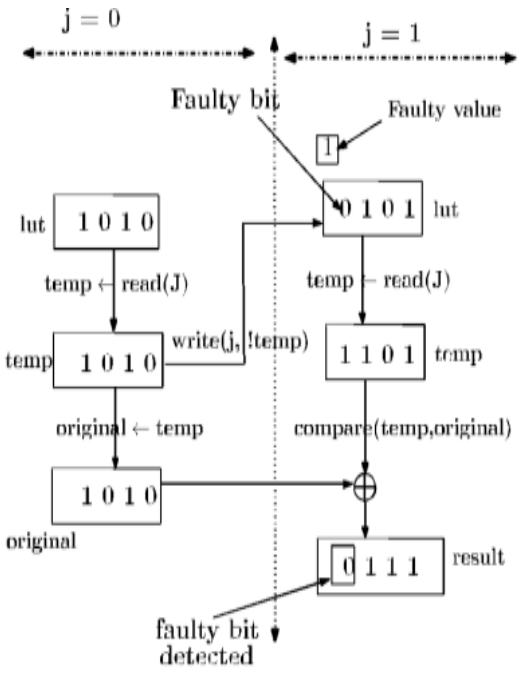


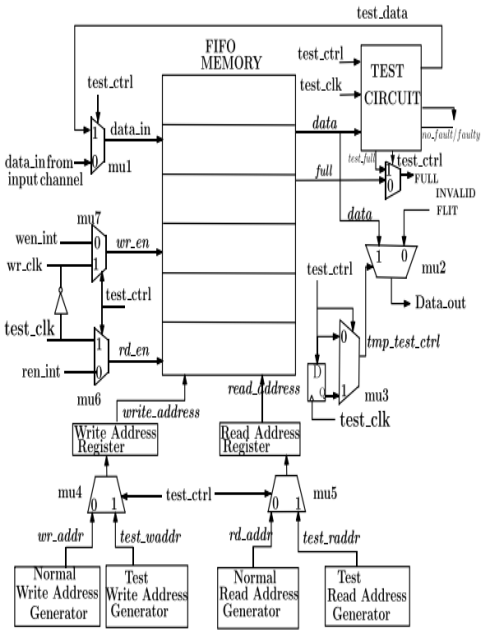
Fig 2 Fault detection during invert phase and restore phase of the transparent SOA-MATS++ test.

Where the XOR of 1010 and 1101 yields a 0 at the MSB position of the result indicating a stuck-at-fault at the MSB position. However, for cases where the initial data for a bit position is different from the faulty bit value, the stuck-at-fault cannot be detected for the bit position after the restore phase of the test. It thus requires one more test cycle to excite such faults.

V. PROPOSED SYSTEM

IMPLEMENTATION OF THE TEST ON FIFO BUFFERS OF NOC ROUTERS.

We present the technique used for implementing the proposed transparent SOA-MATS++test on a mesh-type NoC. Data packets are divided into flow control units (flits) and are transmitted in pipeline fashion. These control units (flits) are assumed to be buffering only at input channels of routers in a mesh type NoC. Thus, for a data traffic movement from one core to another, the online test is performed only on the input channel FIFO buffers, which lie along the path. The buffers operate in two modes, the normal mode and the test mode. The normal mode and test mode of operation of a FIFO buffer are synchronized with two different clocks. The clock used for test purpose (referred as test_clk in this brief) is a faster clock compared with the clock required for normal mode (router clock).



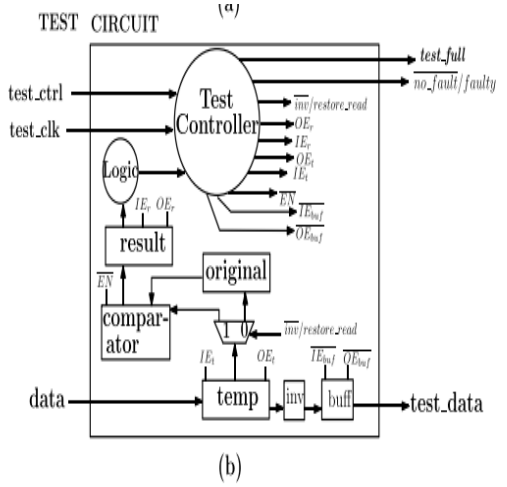


Fig.3. (a) Hardware implementation of the test process for the FIFO buffers. (b) Implementation of test circuit.

The FIFO buffers are allowed to be operative in normal mode for sufficient amount of time before initiating their test process. This delay in test initiation provides sufficient time for run-time intermittent faults developed in FIFO buffers to transform into permanent faults. The test process of a targeted FIFO buffer is initiated by a counter, which switches the FIFO buffer from normal mode to test mode. The switching of FIFO buffers from normal mode to test mode occurs after a certain period of time without caring about the present state of the FIFO buffer. It may be argued that at the instant of switching, the buffer may not be full, and as a result not all locations would be tested during the test cycle. However, test initiation after the buffer gets full would cause the following problems. First, wait for the buffer to get full would unnecessarily delay the test initiation process and would allow faults to get accumulated. Second, test of the entire buffer would prolong the test time and would negatively affect the normal mode of operation.

Test Architecture.

The FIFO buffer present in each input channel of an NoC router consists of a SRAM-based FIFO memory of certain depth. During normal operation, data flits arrive through a data_in line of the buffer and are subsequently stored in different locations of the FIFO memory. On request by the neighboring router, the data flits stored are passed on to the output port through the data_outline. Fig. 3(a) shows the FIFO memory with data_in and data_out line. To perform the transparent SOA-MATS++test on the FIFO buffer, we added a test circuit, few multiplexers and logic gates to the existing hardware, as shown in Fig. 3(a). The read and write operations on the FIFO buffer are controlled by the read enable and write enable lines, respectively. The multiplexers mu6 and mu7 select the read and write enable during the normal and test process. During normal operation when the test_ctrl is asserted low, it provide internal write and read enable lines. However, during test process, the write enable and read enable are synchronized with the test clock. As mentioned earlier, the read and write operations during test are performed at alternate edges of a test clock. The read operations are synchronized with the positive edges, while the write_clk is obtained by inverting the test clock. In test mode (test_ctrl high), the test read and write addresses are generated by test address generators implemented using gray code counters similar to the normal address generation. Muxes m4 and m5 are used to select between normal addresses and test addresses. Consider the situation when the FIFO buffer is in normal mode with flits being transferred from the memory to the data_out line. After a few normal cycles, the test_ctrl is asserted high, switching the buffer to test mode. As long as the buffer is in test mode, no external data is allowed to be written to the buffer, or in other words, the buffer is locked for the test period. As a result, the input data line for the FIFO memory is switched from the external data_inline to test_data line available from the test circuit. At the switching instant, the flit which was in the process of being transferred to the data_outline is simultaneously read into the Test Circuit. However, a one clock cycle delay is created for the flit to move to thedata_outline. This delay ensures that the flit is not lost during the switching instant and is properly received by the router, which requests for it. The single cycle delay in the path of the traveling flit is created by the D-type flip-flop and the multiplexerm3, as shown in Fig. 3(a). The flit, which is read in the test circuit, is stored in a temporary register temp and the test process begins with this flit.

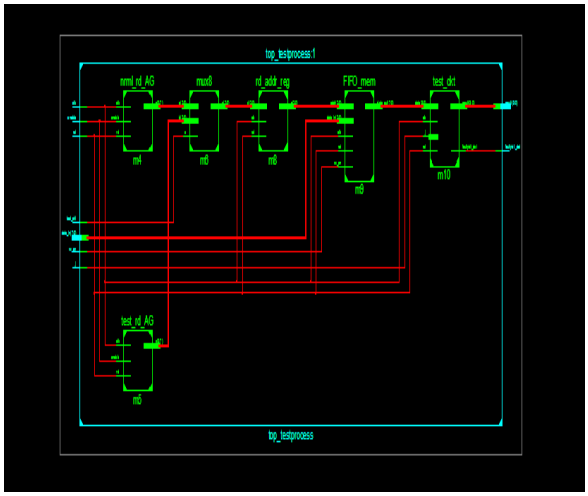
VI. RESULTS

The Verilog HDL Modules have successfully simulate, verified and synthesized using Xilinxise13.2. Proposed Result.

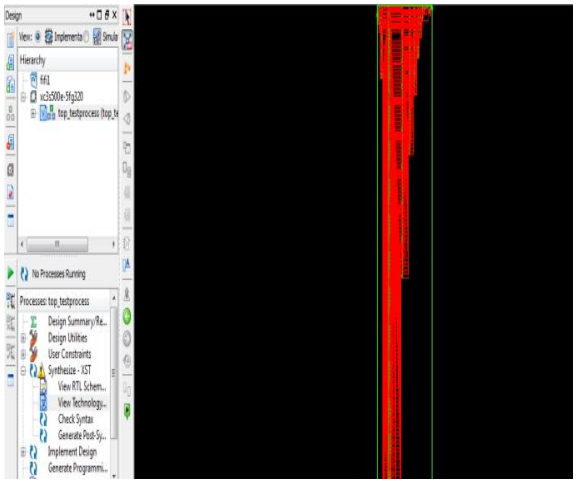
Simulation for Fault detection of 4 bit data:

SYNTHESIS RESULTS:

RTL SCHEMATIC:



TECHNOLOGY SCHEMATIC



DESIGN SUMMARY:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	265	4656	5%
Number of Slice Flip Flops	291	9312	3%
Number of 4 input LUTs	494	9312	4%
Number of bonded IOBs	12	232	5%
Number of GCLKs	2	24	8%

Timing Summary.

```
=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Delay:               5.776ns (Levels of Logic = 3)
  Source:            j (PAD)
  Destination:       faultybit_det (PAD)

  Data Path: j to faultybit_det
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   1.106   0.532  j_IBUF (j_IBUF)
     LUT2:I0->O            1   0.612   0.357  m10/m2/Mxor_result_Result<3>1 (result_3_OBUF)
     OBUF:I->O                 3.169          result_3_OBUF (result<3>)
    ----------------------------------------
    Total                      5.776ns (4.887ns logic, 0.889ns route)
                               (84.6% logic, 15.4% route)

=========================================================================
```

VII. CONCLUSION

In this work, an algorithm is proposed namely transparent SOA-MATS++ test generation to detect run-time permanent faults occurring in SRAM-based FIFO memories. This test can be utilized to perform online and periodic test of FIFO memory present within the routers of the NoC. Periodic testing feature of buffers prevents accumulation of faults and also allows test of each location of the buffer. We have also proposed an online test circuit for the routing logic that is performed simultaneously with the test of buffers and involves utilization of the unused fields of the header flits of the incoming data packets for test pattern encoding. Test circuit designed in the proposed section detects 4 bit faults for an 8 bit data. Results are observed using Xilinx 13.2. Synthesis results show an impact that periodic testing of FIFO buffers doesn't have much effect on the overall throughput of the NoC except when buffers are tested too frequently.

Future Scope: As future work, we would like to modify the proposed FIFO testing technique that will allow incoming data packets to the router under test without interrupting the test.

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BIOGRAPHY:

K. Premlatha is from Hyderabad, Telangana, completed M.tech in ECE with specialization (Digital Systems and Computer Electronics) from JNTUH in 2005. She has completed B.E in EC.E from S.R.K.R Engineering College affiliated by Andhra University in 2000. Currently she is working as an Associate Professor in ECE Department at Shadan Women's College of Engineering & Technology, Hyderabad from 2005. Her areas of Research interest include Low Power VLSI, Digital Systems Design, Design for Testability.