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AN EFFICIENT FPGA IMPLEMENTATION OF SHIFT REGISTER USING PULSED LATCHES

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Abstract: This paper proposes a low-power and area-efficient shift register exploitation digital pulsed latches and power consumption are reduced by commutation flip-flops with pulsed latches. This methodology solves the temporal arrangement downside between pulsed latches through the utilization of multiple non-overlap delayed pulsed clock signals rather than the traditional single pulsed clock signal. The register uses a little variety of the periodic clock signals by grouping the latches to many sub shifter registers and exploitation further temporary storage latches. In digital circuits, a register could be a cascade of flip-flops, sharing constant clock, during which the output of every flip-flop is connected to the "data" input of successive flip-flop within the chain, leading to a circuit that shifts by one position the "bit array" hold on in it, 'shifting in' the information present at its input and 'shifting out' the last bit within the array, at every transition of the clock input. Usually, a register is also flat, specified its "data in" and stage outputs square measure themselves bit arrays: this is often enforced just by running many shift registers of constant bit-length in parallel. Extension of the project is using SRAM. The design process done in the proposed is implemented using SRAM.

Keywords*:* Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register

I. Introduction

Flip flops are the basic storage elements used extensively in all kinds of digital designs. As the feature size of CMOS technology process scaled down according to Moore's Law, designers are able to integrate many numbers of transistors onto the same die. The more transistors there will be more switching and more power dissipated in the form of heat or radiation. Heat is one of the phenomenon packaging challenges in this epoch, it is one of the main challenges of low power design methodologies and practices. Another driver of low power analysis is that the responsibleness of the computer circuit. Additional switch implies higher average current is expelled and so the chance of responsibleness problems occurring rises. We have a tendency to area unit moving from laptops to tablets and even smaller computing digital systems. With this profound trend continued and while not a match trending in battery lifetime, the additional low power problems can have to be compelled to be addressed, the present trends can eventually mandate low power style automation on a awfully giant scale to match the trends of power consumption of today's and future integrated chips. Power consumption of terribly giant Scale Integrated style is given by

Generalized relation, P = CV2f. Since power is proportional to the sq. of the voltage as per the relation, voltage scaling is that the most distinguished thanks to scale back power

dissipation. However, voltage scaling is leads to threshold voltage scaling that bows to the exponential increase in discharge power.

Though several contributions have been made to the art of single edge triggered flip-flops, a need evidently occurs for a design that further improves the performance of single edge triggered flip flops patterns. The architecture of a shift register is quite simple. An N-bit register consists of series connected N information flip-flops. The speed of the flipflop is a smaller amount necessary than the realm and power consumption as a result of there's no circuit between flip-flips within the register. The tiniest flip-flop is appropriate for the register to scale back the realm and power consumption.

Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flipflop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

II. Shift Registers

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers and image processing ICs Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs.

An image-extraction and vector generation VLSI chip uses a 4K-bit register A 10-bit 208 channel output LCD column driver IC uses a 2K-bit register A 16- megapixel CMOS image detector uses a 45K-bit register.

As the word length of the shift register will increase, the world and power consumption of the register become necessary style issues. The smallest flip-flop is appropriate for the register to cut back the world and power consumption. Recently, pulsed latches have replaced flip flops in several applications, as a result of a pulsed latch is way smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

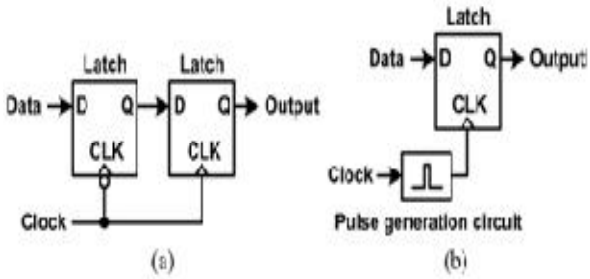


Figure 1: (a) Master-slave flip-flop. (b) Pulsed latch**.**

This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. Shift registers can have both parallel and serial inputs and outputs.

These are often configured as 'serial-in, parallel-out' (SIPO) or as 'parallel-in, serial-out' (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also 'bidirectional' shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register' previous work often measured energy consumption using a limited set of data patterns with the clock switching every cycle. But real designs have a wide variation in clock and data activity across different TE instances.

For example, low power microprocessors build intensive use of clock gating leading to several TEs whose energy consumption is dominated by input file transitions instead of clock transitions. Other TEs, in distinction, have negligible information input activity however are clocked each cycle. Shift registers, like counters, are a variety of successive logic. Successive logic, not like combinatory logic isn't solely full of this inputs, but also, by the previous history. In alternative words, successive logic remembers past events. Pulsed latch structures use associate degree edge-triggered pulse generator to supply a

brief transparency window. Compared to master–slave flip-flops, pulsed latches have the benefits of requiring only 1 latch stage per clock cycle and of permitting time-borrowing across cycle boundaries.

The major disadvantages of pulsed latch structures are the inflated condition to temporal arrangement hazards and therefore the energy dissipation of the native clock pulse generators.

III. Proposed Architecture

A master-slave flip-flop using two latches in Fig.1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

The pulsed latch cannot be employed in shift registers because of the temporal arrangement downside, as shown in Fig. 2. The shift registers in Fig. 2(a) consists of many latches and a periodic clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the temporal arrangement downside within the shifter register. The output of the primary latch (Q1) changes properly as a result of the input signals of the primary latch (IN) is constant throughout the clock pulse breadth (TPULSE).But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

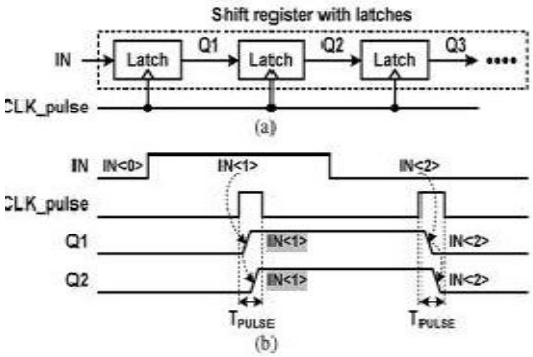


Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b)Waveforms

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power over heads.

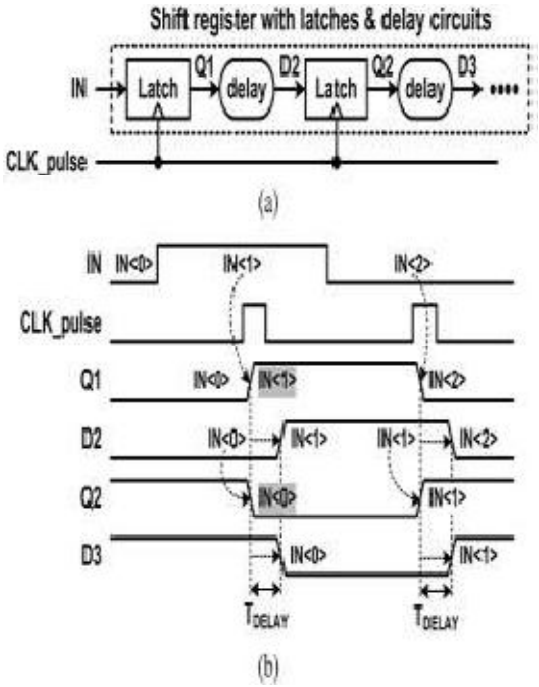
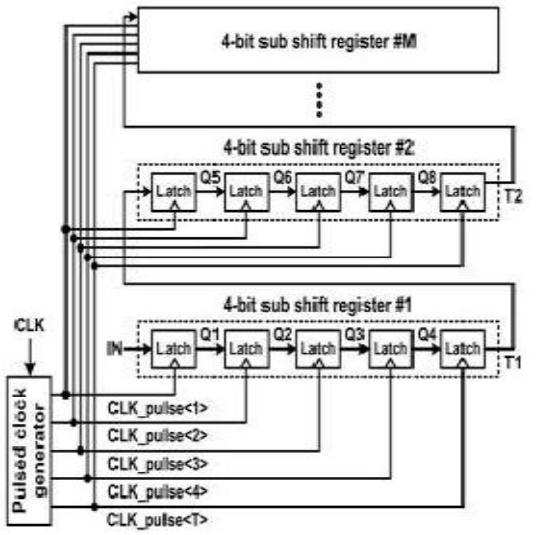
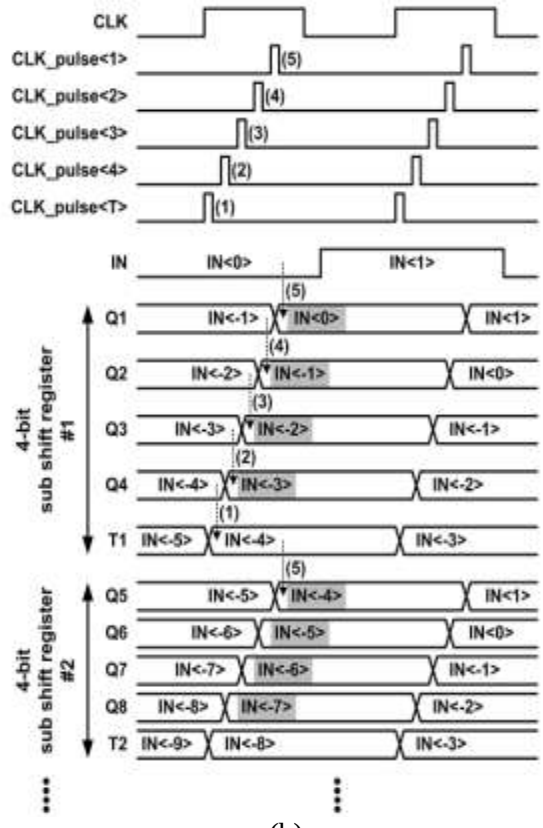


Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic. (b)Waveforms

A 4-bitsub shifter register consists 5 of 5 latches and it performs shift operations with five non overlap delayed periodical clock signals (CLK_pulse<1:4>andCLK_pulse<T>). within the 4-bit sub shift register #1, four latches store 4- bit knowledge (Q1-Q4) and therefore the last latch stores 1-bit temporary knowledge (T1) which is able to be hold on in the initial latch (Q5) of the 4-bit sub register #2. Fig. 4(b) shows the operation waveforms within the proposed register.



(a)



(b)

Fig. 4. Proposed shift register. (a) Schematic. (b) Waveforms.

The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register is selected by considering the area, power consumption, speed.

Area optimization: The area optimization can be performed as follows. Whenthe circuit areas are normalized with a latch, the areas of a latchand a clock-pulse circuit are 1 and , respectively. The total area becomes$(\alpha_A \times (K+1) + N\left(1+\frac{1}{K}\right)$. The optimal $K(=\sqrt{N/\alpha_A})$for the minimum area is obtained from the first-orderdifferential equation of the total area $(0=\alpha_A - N/K)$.An integer for the minimum area is selected as a divisor of, which is nearest to $\sqrt{N/\alpha_A}$.

Power optimization: The power optimization is similar to the area optimization. The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are1 and, respectively. The total power consumption is also $(\alpha_p \times (K+1) + N\left(1+\frac{1}{K}\right)$ .An integer for the minimum power is selected as a divisor of, which is nearest to $\sqrt{N/\alpha_p}$.

Chip Implementation: The maximum clock frequency within the standard register is restricted to solely the delay of flip-flops as a result of there's no delay between flip-flips. Therefore, and power consumption are additional necessary than the speed for choosing the flip-flop. The projected register uses latches rather than flip-flops to scale back the realm and power consumption.

IV. Extension:

SRAM is a type of semiconductor memory which is volatile in nature (retains the data as long as power is being supplied).It performs both read and write operations to store and fetch the data, based on the particular address. The read and write operations are controlled by the word line. Based on the bit line condition the data in it is stored and consists of a 1bit latch to store the data.

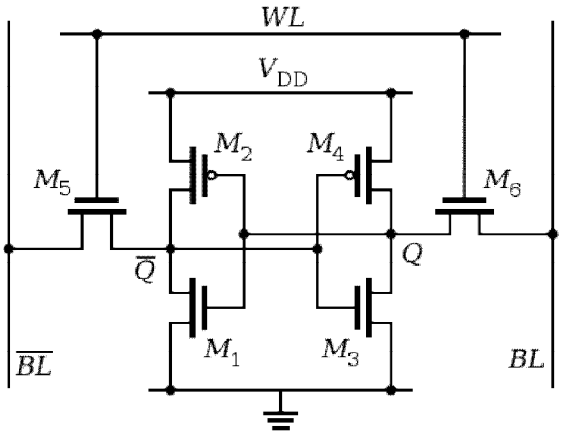


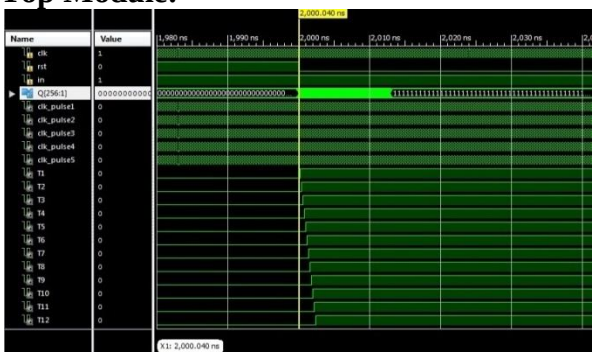
Fig. 5. 6T SRAM

The 256bit periodic latch register is employed as a part of SRAM so as to store the info in SRAM and fetch the info in step with the given address location. So it's low power consumption than the memory with general latch.

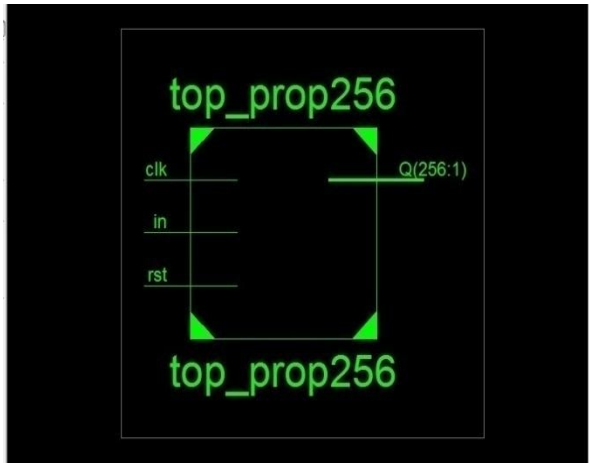
V. Results

Proposed result:

Top Module:



RTL Schematic:



Design Summary:

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	186	4656	3%
Number of Slice Flip Flops	322	9312	3%
Number of 4 input LUTs	5	9312	0%
Number of bonded IOBs	259	66	392%
Number of GCLKs	6	24	25%

Timing Report:

```
Data Path: m65/m1/Q_1 to Q<253>
                              Gate     Net
  Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name
  ----------------------------------------  ------------
   FDR:C->Q             1   0.514    0.357  m65/m1/Q_1 (m65/m1/Q_1
   OBUF:I->O                3.169           Q_253_OBUF (Q<253>)
  ----------------------------------------
  Total                    4.040ns (3.683ns logic, 0.357ns route
                                   (91.2% logic, 8.8% route)
```

VI. CONCLUSION

This paper projected a low-power and area-efficient register victimization pulsed latches. The register reduces area and power consumption by work flip-flops with pulsed latches. In this paper proposed shift register saves 37% area and 44% power when compared to conventional shift register with flip-flops. The temporal order drawback between pulsed latches is resolved victimization multiple non-overlap delayed pulsed clock signals as an alternate of one periodic clock signal.

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