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DESIGN OF REVERSIBLE 32-BIT BCD ADD-SUBTRACT UNIT USING PARALLEL PIPELINED METHOD

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Abstract:

This paper proposes the design of 32-bit Binary Coded Decimal (BCD) addition and subtraction unit using reversible logic gates. The reversible 32 -bit BCD addition unit is designed using the following modules such as reversible 4-bit Carry Propagate unit using reversible logic gates such as Feynman gate and URG gate and a reversible 4-bit error correction unit. The reversible 32-bit BCD subtraction unit is designed based on the nine's complement method of 4-bit reversible BCD addition. In BCD subtraction unit, the error correcting block is designed with the conditional reversible logic COG gate to make the necessary corrections at the output to get exact output. The reversible 32- bit BCD addition and subtraction unit is designed based on the parallel pipelined unit to enhance the speed of operation. This proposed reversible 32-bit BCD addition module has 416 garbage values with the critical path delay of 17.420 ns; reversible 32-bit BCD subtraction module has 240 garbage values with the critical path delay of about 17.420 ns.

Index Terms— Reversible logic gates; BCD adder; BCD subtractor, Reversible add-subtract unit.

I. INTRODUCTION

The growing technologies have increased the demand of high performance computing. According to G. Moore's low, number of transistor counts to be integrated per unit area in devices will almost double in one and half year. To achieve high speed computation, high packaging density in the logic circuits is required which results in more heat dissipation. The conventional computing is found unable to deal with low power, high compaction and heat dissipation issues of the current computing environment. Reversible Computing is one way to overcome the problem of heat dissipation in computing chips which in turn help in increasing the packaging density. Reversible Logic seems to be hopeful due to its wide application in emerging technologies such as quantum computing, optical computing and power efficient nanotechnologies etc. Reversible circuits do not lose information. A reversible logic gate has one to one mapping between input and output vectors .

Reversible logic is the effective alternative in the design of low power arithmetic unit. The reversible logic gate, which has one to one mapping technology

provide output with zero loss of information. In reversible logic gates input vectors can be retrieved from the output vectors with accuracy and low power dissipation. BCD employed on various digital processors decreases the delay of manipulation. BCD circuit may open new application areas of finance, commerce, land management and internet-based systems. BCD digit eliminates the truncation error and thereby reduces the computation delay. In this paper, BCD addition and subtraction unit has been implemented using the reversible logic gates. The addition and subtraction unit is designed for 32-bit input data using reversible logic gates. BCD adder and subtraction requires error correction unit which provides exact BCD output.. This proposed method will effectively reduce the delay, error and garbage values.

A. Reversible logic

Reversible logic gates are designed to meet the needs such as high speed, no loss of data in the form of heat energy. These gates have stretched its application over wide range such as low power optical computing, nanotechnology and quantum computing. One to one mapping of input and output vectors of reversible logic gates prevents the gate from loss of information in the form of heat energy. Reversible logic gates reduce the loss of information when repossessing the input vectors from output vector. Input vectors of the reversible logic gates are 0‟s and 1‟s; the output vectors comprise of output values and the garbage values. These garbage values along with output values helps in retrieving the input vectors without any loss in information. Reversible logic gates are more effective in implementing the Boolean expressions with high accuracy. This paper proposes the design of BCD adder and subtraction for 32-bit input data using reversible logic gates.

II.BASICS OF ALL OPTICAL REVERS IBLE LOGIC

Reversible logics are implemented with optical technology using some building blocks such as MZI based optical switch, beam splitter and beam combiner.

SOA Based MZI Switch An SOA based MZI switch can be de signed using two Semiconductor Optical Amplifiers (SOA-1, SOA-2) and two couplers (C -1, C-2) [8], [9]. In an MZI switch, there are two inputs ports A and B, and two output ports called bar port and cross port, respectively, as shown in Figure 1 and 2.

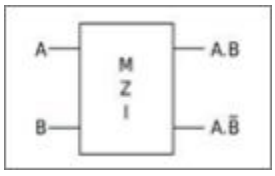

Fig. 1. Block diagram of Mach-Zehnder Interferometer switch

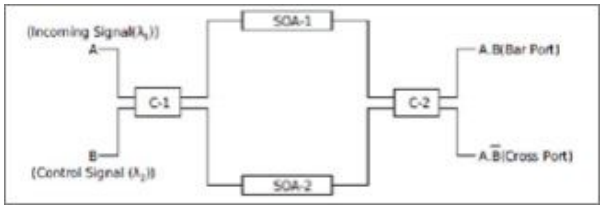

Fig. 2. SOA based Mach-Zehnder

Interferometer switch [8] The optical signal at port B is termed as the control signal and signal at port A is termed as incoming

signal. When there are signals present at port A and port B then there is a presence of light signal at the bar port an d absence of light signal at the cross port. In the absence of co ntrol signal at port B and presence of incoming signal at port A, the outputs of MZI are interchanged and results in the presence of light at the cross port and no light at the bar port. Here, absence of light is considered as the logic value 0 and presence of light is considered as logic value 1. This behavior of SOA based MZI switch can be written as Boolean functions having inputs to outputs mapping as (A, B) → (P=A.B, Q = A.B), where A, B are the inputs and P, Q are the outputs of MZI, respectively. The optical cost and the delay ( ) of MZI based all optical switch is considered as unity. The authors have considered the following optimization parameters for the all-optical reversible logics: optical cost i.e. number of MZI switches, number of BC and BS used in the logic circuit, and optical delay i.e. number of stages of MZI switches used in the design of logic circuit. All-optical Feynman gate: The Feynman gate (FG) has mapping (A, B) → (P=A, Q=A⊕B) where A, B are the inputs and P=A, Q=A⊕B are the outputs, respectively. The Feynman gate can be realized using 2 MZI switches, 2 bea m combiners (BC) and 3 beam splitters (BS) in all optical domain as shown in figure 3.

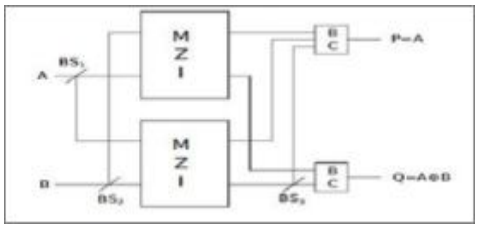

Fig. 3. Feynman gate and its all optical implementation

III. PROPOSED DESIGN

In this paper, reversible logic gates are used to realize the 32-bit BCD addition and subtraction units. Reversible logic gates are employed so as to reduce the delay and power dissipation in the BCD arithmetic unit. BCD adder adds two input data and produces the sum as the result. On account of any error in the sum value like the output data so generated is not a BCD number then there needs a correction block for the error output so produced [7]. Reversible BCD subtraction unit subtracts the two input values and generates the difference value as the output. In the proposed design, subtraction is realized by taking the nine‟s complement and adding the complemented value along with the other input data [8].

A. Reversible 32-bit BCD Addition

Reversible BCD addition design consists of two modules such as 4-bit addition unit and an error correcting unit.

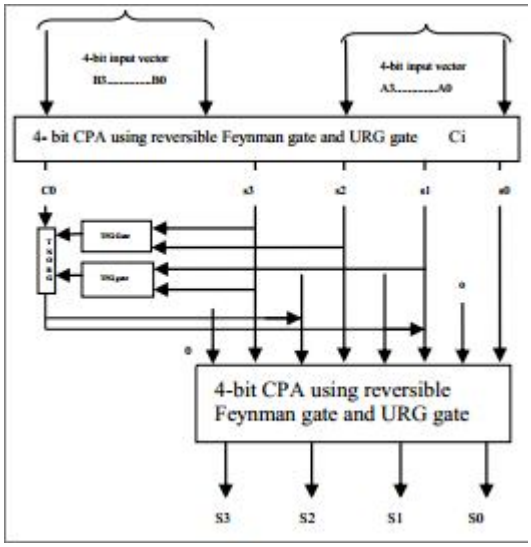

Fig. 4. Proposed 4-bit reversible BCD Addition unit

Reversible 32-bit BCD addition unit is realized by cascading eight 4- bit BCD adder along with the error correction unit designed individually in the Carry Propagate adder (CPA) fashion. Reversible logic gates used in this designing are Feynman gate and URG gate for about 4-bit input vectors. Fig.4, shows the design of proposed 4-bit BCD addition unit using reversible logic gates. The generated output from 4-bit adder unit is checked for error using error correction unit. Error correction block is designed by (4x1) MUX using Toffoli gate and TNORG gate. If the output of (4x1) MUX is „1" then the value of binary „0110" is added with the output of stage 1 of reversible 4-bit BCD adder; else the output is generated without any correction.

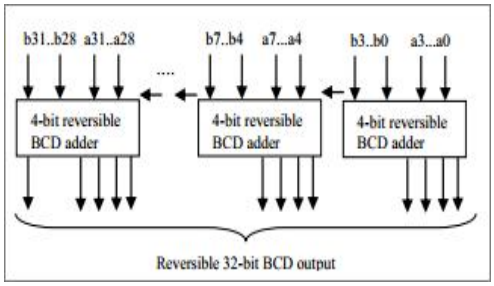

Fig. 5. Proposed reversible 32-bit BCD adder

By cascading 8 reversible 4-bit BCD adder along with the error correction block, 32-bit reversible BCD addition can be realized as shown in Fig. 5

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B. Reversible 32-bit BCD Subtractor

Reversible 32-bit BCD subtraction unit is designed based on addition of nine"s complement of one of the two 4-bit inputs and is added with the other 4-bit input value.

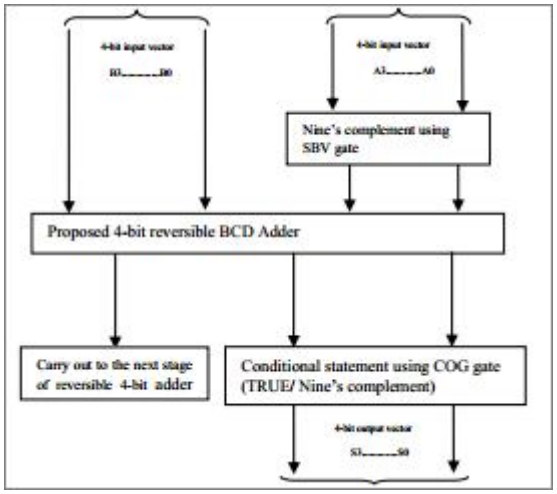


Fig. 6. Proposed 4-bit reversible BCD Subtract unit

Fig. 6, the error correction block is designed for individual 4-bit BCD addition blocks. Reversible 4-bit addition unit is designed based on CPA fashion using the reversible logic gates such as Feynman gate and URG gate; error correcting unit is designed using the reversible logic gates such as Toffoli gate and TNORG gate. Nine"s complement of one of the 4-bit input vectors is designed using reversible SBV gate. In case

of the output of 4-bit BCD adder design provides the carry of „1" the output of the particular block is fed into the nine"s complement; else if the carry is „0" the output of 4-bit BCD adder is generated at the output vector with no correction made at the error correction unit. In case of any error correction required for the output of reversible 4-bit BCD subtraction unit the reversible COG gate plays the role conditional statement; if no correction is needed then the output of reversible 4-bit subtraction unit is generated without any correction.

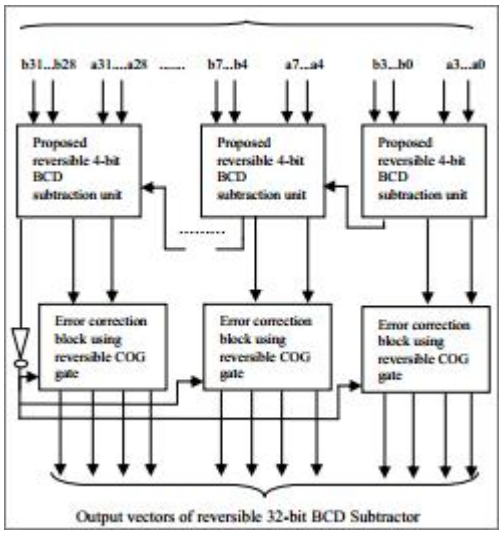


Fig. 7. Proposed 32-bit reversible BCD Subtract unit

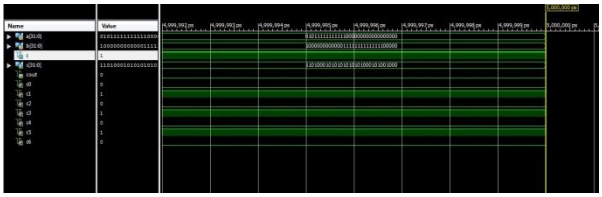
From Fig. 7, it is inferred that the 32-bit BCD subtraction is realized by cascading of eight 4-bit reversible BCD subtraction units along with the error correction block manipulated for individual reversible 4-bit BCD subtraction.

IV. CONCLUS ION

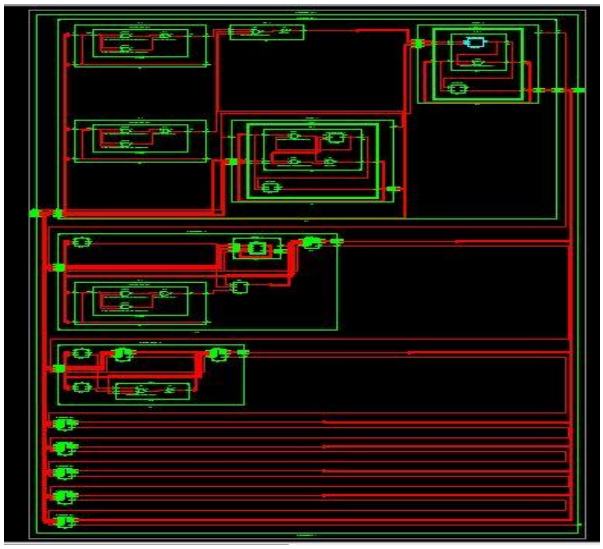
In this paper, the design of 32-bit BCD add- subtract unit have been implemented using reversible logic gates. Modules such as 4-bit BCD addition, error correction unit, (4x1) MUX, conditional statements, 4-bit nine"s complement unit have been designed using the reversible logic gates. BCD arithmetic units are speedy manipulation with reduced area. The four bit BCD addition is designed in the CPA fashion to further enhance the speed of 32-bit BCD arithmetic design for add- subtract units. 32-bit subtraction unit have been designed using 4-bit nine"s complement and 4- bit BCD addition unit. The proposed module has wide range of application in digital signal processing. The estimated parameters for reversible 32-bit BCD addition unit is about 416 garbage values with the critical path delay of 17.420 ns; reversible 32-bit BCD subtraction module is about 240 garbage values with the critical path delay of about 17.420 ns.

IV. SIMULATION RESULT

Reversible 32 bit Adder Simulation



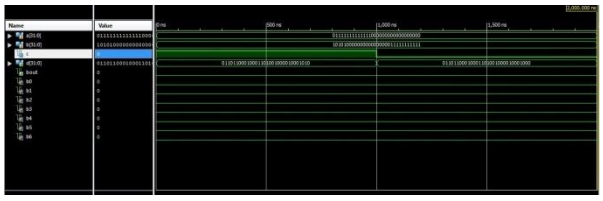
Reversible 32 bit Adder rtl schematic.



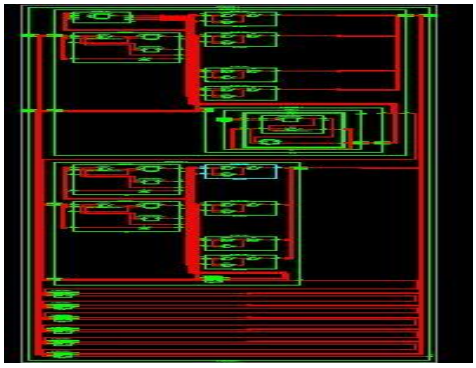
Reversible 32 bit Adder design summary.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	64	960	6%
Number of 4 input LUTs	112	1920	5%

Reversible 32 bit Subractor Simulation



Reversible 32 bit Subractor rtl schematic



Reversible 32 bit Subractor design Summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	81	960	8%
Number of 4 input LUTs	144	1920	7%

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