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SOFT-SWITCHING ANALYSIS OF FULL-BRIDGE PWM DC–DC CONVERTER WITH CONTROLLED OUTPUT RECTIFIER USING TURN-OFF SNUBBER

[1]SANKARASETTY NAGARJUNA, [2]K.SURESH
[1]M.Tech, NALANDA INSTITUTE OF ENGINEERING & TECHNOLOGY
[2]Associate professor, NALANDA INSTITUTE OF ENGINEERING & TECHNOLOGY

ABSTRACT- In this project we are implementing a full bridge pulse-width modulated dc-dc converter with the controlled secondary side rectifier by utilizing the novel non dissipative energy recovery turn-off snubber and also an innovative control algorithm to achieve soft switching. Therefore in this project we are presenting a zero-voltage and zero-current switching full-bridge pulse-width modulated dc–dc converter with controlled secondary side rectifier using a novel non dissipative energy recovery turn-off snubber. By utilizing a turn-off snubber, controlled rectifier with the innovative control algorithm and the circulating current of the converter which have been eliminated and also the soft switching for all power switches of the inverter is achieved for full-load range from no-load to short circuit. Therefore by using the simulation results we can analysis the principle of converter operation on 4.5 kW, 100 kHz model of the converter which is present in this project. By using the simulation results we can analyze the proposed method.

Index Terms—Controlled output rectifier, dc–dc converter, snubber circuit, soft switching, zero-voltage zero-current switching (ZVZCS).

INTRODUCTION

The conventional phase shifted PWM converters are often used in many applications because their topology permits all switching devices to operate with soft switching by using circuit parasitics such as power transformer leakage inductance and devices junction capacitance. In very used phase-shifted PWM control converters, circulating current flows through the power transformer and switching devices during freewheeling intervals. To achieve high efficiency of these converters, it is necessary to reduce switching losses and conduction losses caused by circulating currents. Generally, the reduction of both mentioned losses can be solved by choice of converter topology, design of a proper control algorithm, and by using appropriate additional circuits. In very used phase-shifted PWM control converters, circulating current flows through the power transformer and switching devices during freewheeling intervals.

Conduction losses of conventional softswitched converter are relatively high due to the circulating current flowing through the primary and secondary windings of the high-frequency transformer during freewheeling period. Moreover, converters need a large commutating current in order to ensure zero-voltage switching (ZVS) operation. Various active or passive, dissipative or non dissipative snubbers, clamps and auxiliary circuits are often added on secondary or primary side of the transformer to ensure soft switching of the main switches and suppression of converter circulating currents [1]–[8]. Diode output rectifier is mostly employed on the secondary side of the power transformer to rectify high frequency secondary voltage. Disconnection of the secondary windings is mostly achieved by application of the reverse bias for the output uncontrolled rectifier (see Fig. 1).

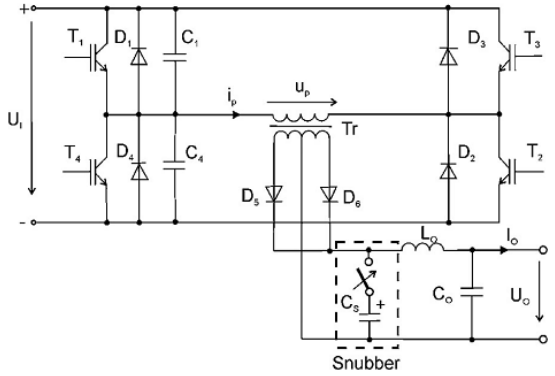


Fig. 1. Principle of the ZVZCS PS-PWM converter operation.

Thus, the RMS current of the transformer and switches are considerably reduced. The features of these configurations are quite well known and widely described in many papers in past decades, e.g. [1]–[8]. It is impossible to present advantages and disadvantages all of them in detail in this paper.

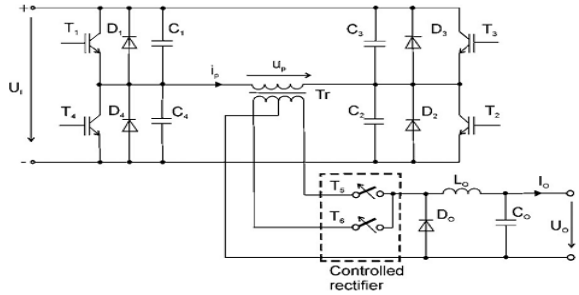


Fig. 2. Principle of the ZVS converter with a controlled rectifier.

But generally, the main drawbacks of these PWM and PS-PWM dc–dc converters dwell in the fact that either reduction of the circulating currents is insufficient or auxiliary circuits are too complex or control algorithms are overcomplicated. Moreover, soft switching is often achieved only in a relatively narrow range of the load. The other and very effective way, how to decrease circulating currents in the converter and, at the time, to achieve reduction of switching losses, is to utilize a controlled output rectifier.

The principle is shown in Fig. 2. Full-bridge inverterT1−T4 is controlled with constant switching frequency and 50% duty cycle and thus cannot control the output voltage or current value. Value of the output voltage or current is controlled via the phase shift between the inverter switchesT1−T4and switches T5 andT6 on secondary side of a high-frequency power transformer. In the all known converters with controlled output rectifier described, the primary IGBTs operate under ZVS. But at ZVS, switching conditions for IGBTs are not very satisfactory because of tail current problems. Moreover, at turn off of the primary transistors, the snubber capacitors in parallel with switches (or transistor output capacitances only) oscillate with parasitic inductances of the input source and wires in a loop with very low dumping.

This increases electromagnetic interference in the converter. In addition, it is complicated to design snubber capacitors for primary transistors for a wide load range. Therefore, ZVS is usually lost at light load and at no-load in these converters, which consequently lead to over current at turn on of the primary switches.

CONVERTERCIRCUITDESCRIPTION

The proposed dc–dc converter shown in Fig. 3 consists of a high-frequency IGBT full-bridge inverter, a center-tapped power planar transformer, a controlled output rectifier, an output LC filter, and a novel type of secondary snubber. The main part of the converter is a high-frequency full-bridge inverter consisting of four fast IGBTsT1−T4and freewheeling diodesD1−D4. The high-frequency center-tapped step-down power transformer Tr with very low leakage inductance is used to transform high frequency voltage of the inverter. The secondary winding of the high-frequency step-down power transformer Tr is connected through a controlled rectifier consisting of series connection of MOSFET and diode (T5,D5;T6,D6)to the output filter. The output filter consisting of smoothing choke LO and capacitor CO serves for smoothing out of the rectified voltage. Control pulses for the full-bridge inverterT1−T4 are very simple. They have constant switching frequency and no phase shift between legs of the inverter. So, the inverter operates approximately with 50% constant duty cycle and thus cannot influence the output voltage value. Value of the output voltage or current is controlled by PWM of output rectifier (see Fig. 4). The control pulses for an output rectifier start simultaneously with the pulses for opposite pair of the primary switches (e.g., pulses forT5start simultaneously with pulses forT3andT4). The length of the secondary control pulses is changed from T to T/2 (dead times are neglected). It means that secondary switches are turned OFF prior to corresponding pairs of primary switches (e.g.,T5 prior toT1 and T2). As a result, the secondary and also primary current of the transformer drops to zero. Only magnetizing current flowing through the primary winding of the transformer is later turned OFF by primary transistors and thus ZC turn-off is achieved.

The primary transistors (T3andT4)are turned ON and active energy from primary side of the converter is transferred through opened secondary transistorT6 to the load. It means that in this way of controlling the rms value of the secondary transistor current is considerably reduced and, consequently, conduction losses are decreased. The new snubber circuit significantly minimizes the turn-off losses of the secondary transistors. The semiconductor switches T5 andT6 on the secondary side of the transformer are used to reset secondary and simultaneously also primary circulating current. The energy stored in the leakage inductance of the power transformer is transferred to the load.

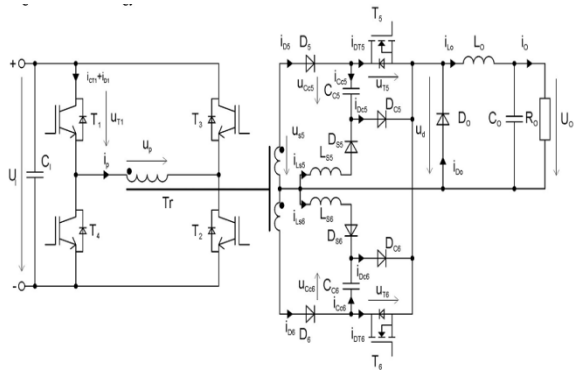


Fig. 3. Scheme of the proposed converter.

OPERATIONPRINCIPLE ANDSNUBBERDESIGN

A. Operation Principle of the Converter

In this section, the basic operation of the proposed converter is described. It is assumed that all switching devices and passive components are ideal. The switching diagram and operation waveforms for

rated load are shown in Fig. 4 and operation analysis of the converter in Fig. 5(a)–(g). The dc–dc converter is controlled by the proposed modified PWM with variable length of the pulses for secondary switches.
Interval(t0–t1): The secondary transistorT5is turned ON at t0 half-period earlier than primary transistors T1 and T2.The capacitorCC5starts discharging through T5,LO,RO,LS5, and DS5. CapacitorCC5 current and voltage time waveforms are as follows:

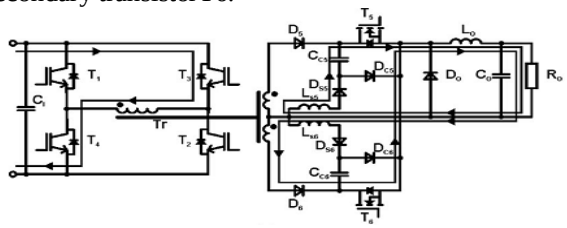
$$i_{Cc5}(t) = \sqrt{\frac{C_{C5}}{L_{S5}}}\left(\frac{U_1}{n} - U_{Cc5}\right)\sin\left(\frac{t-t_0}{\sqrt{L_{S5}C_{C5}}}\right) \quad (1)$$

$$u_{Cc5}(t) = \frac{U_1}{n} + \left(U_{Ce5} - \frac{U_1}{n}\right)\cos\left(\frac{t-t_0}{\sqrt{L_{S5}C_{C5}}}\right) \quad (2)$$

From (2), it follows that total discharging of the capacitor occurs only in the case if its initial voltageUCc5 is higher than double rectified voltage $u_d = U_I ln$

$$\frac{U_1}{n} + \left(U_{Ce5} - \frac{U_1}{n}\right)(-1) \le 0 \rightarrow U_{Cc5} \ge 2\frac{U_I}{n} \quad (3)$$

The rate of rise of discharging current of the capacitorCC5 is limited by the snubber inductanceLS5, and thus zero current turn on for the transistor T5 is achieved. At the same time, transistors T3 andT4 are turned ON. Because the transistorT6 is already in on-state, so the output voltage of the rectifier ud is equal to UI/n(where n=up/us is transformer turn's ratio). The discharging current of capacitorCC5reduces the current of the primary transistorsT3,T4, and the current of the secondary transistorT6.



(a)

Fig. 4. (a) Operation in intervalt0−t1.

If condition (3) is valid, capacitor discharging time (when uCc5(t)=0) can be obtained from (2) as follows:

$$t_{Cc5dch} = t_1 - t_0 = \sqrt{L_{S5}C_{C5}}\, arccos\left(\frac{\frac{U_1}{n}}{\frac{U_1}{n} - U_{Cc5}}\right) \quad (4)$$

Discharging time is from interval

$$\frac{\pi}{2}\sqrt{L_{S5}C_{C5}} < t_{Cc5dch} \le \pi\sqrt{L_{S5}C_{C5}} \quad (5)$$

As discharging time is greater than quarter of resonance period, the magnitude of the discharging current of the capacitor can be derived from (1) as follows:

$$I_{Cc5dch} = \left|\sqrt{\frac{C_{C5}}{L_{S5}}}\left(\frac{U_1}{n} - U_{Cc5}\right)\right| = \sqrt{\frac{C_{C5}}{L_{S5}}}\left(U_{Cc5} - \frac{U_1}{n}\right) \quad (6)$$

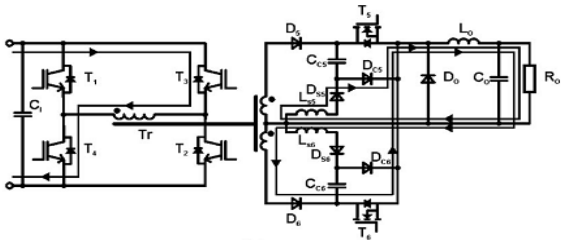
Interval (t1−t2): The energy stored in snubber inductance LS5is now transferred through DS5,DC5,LO,RO, andLS5. The snubber inductor current decays to zero according to equation:

$$i_{Ls5}(t) = \sqrt{U_{Cc5}\left(U_{Cc5} - \frac{U_1}{n}\right)}\sqrt{\frac{C_{C5}}{L_{S5}}} - \frac{U_1}{n}\frac{t-t_1}{L_{S5}} \quad (7)$$

From this equation, decay time of the inductor current can be determined

$$t_{Cc5dch} = t_1 - t_0 = \sqrt{\frac{U_{Cc5}\left(U_{Cc5} - 2\frac{U_1}{n}\right)\sqrt{\frac{C_{C5}}{L_{S5}}}}{\frac{U_1}{n}}}\, L_{S5} \quad (8)$$

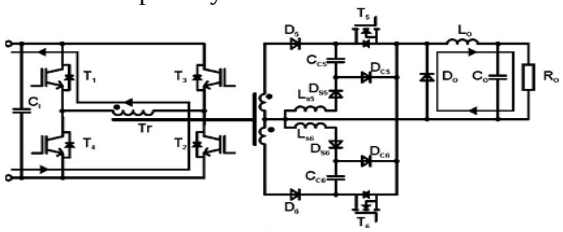
Att2, the whole load current flows through the transistorT6.



(b)

(b) Operation in intervalt1−t2.

Interval t3−t4: This interval starts with the turn off of the primary transistorsT3 andT4.

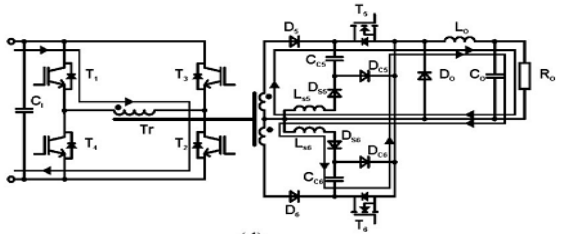


(c)

(c) Operation in intervalt3−t4

The magnetizing current of the transformer Tr discharges the output capacitances COSS of the transistors T1 and T2 and charges the output capacitances of the transistorsT3andT4. If we assume that magnetizing inductance of the power transformer and the output smoothing inductance are much greater

Interval t4−t5: After turn on of the transistorsT1,T2, and T6,att4, commutation from the freewheeling diode DO to the transistorT5occurs.



(d)

(d) Operation in intervalt4−t5

Collector current of the transistor T5 is reduced by the discharging current of the capacitor CC6 through the opposite transistor T6 to load and later, after commutation to diodeDC6, by the current of the inductance LS6. The rate of rise of the collector current of the secondary transistor T5 is limited by the leakage inductance referred to secondary side of the transformer

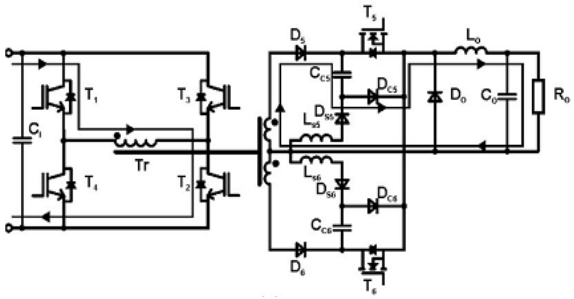
$$\frac{di_{DT5}}{dt} = \frac{U_1}{n} \cdot \frac{1}{(L'_{1\sigma}+L_{2\sigma})} \quad (9)$$

The rate of rise of the collector current of the primary transistorsT1andT2is primarily limited by the leakage inductance referred to the primary side of the transformer

$$\frac{di_{CT1,CT2}}{dt} = \frac{U_1}{(L_1H+L_{1\sigma})} + \frac{U_I}{L_{1\sigma}+L'_{2\sigma}} \quad (10)$$

The leakage inductance acts for secondary and primary transistors as a turn-on snubber.

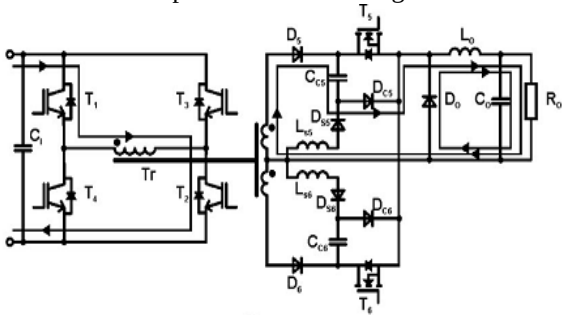
Interval t5−t6: At t5, the secondary transistorT5turns off. Its current commutates to the capacitorCC5and the diodeDC5and consequently zero voltage turn off of this transistor is ensured. The energy of the leakage inductance of the power transformer is absorbed by the snubber capacitanceCC5and by the load.



(e)

(e) Operation in interval t5−t6.

Interval t6−t7: At t6, the rectified voltage ud reached zero and afterward the waveform of the charging process of the ca pacitorCC5 are changed.



(f)

(f) Operation in intervalt6−t7.

In this interval, the whole energy of the leakage inductance is absorbed by the capacitorCC5only. Charging current of the capacitor can be expressed as

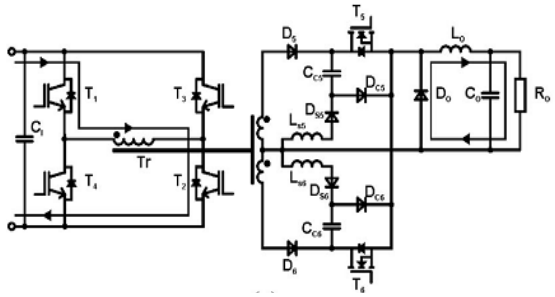
$$i_{Cc5}(t) = i_{Cce(t_6)} \cos\left(\frac{t-t_6}{\sqrt{C_{c5}L'_\sigma}}\right) + \left(\frac{U_1}{n} - u_{Cc5(t_6)}\right)\sqrt{\frac{C_{c5}}{L'_\sigma}} \sin\left(\frac{t-t_6}{\sqrt{C_{c5}L'_\sigma}}\right) \quad (11)$$

where $L'_\sigma = L'_{1\sigma} + L_{2\sigma}$ leakage inductance of the transformer referred to the secondary side;

$L'_{1\sigma}$ leakage inductance of the primary winding referred to the secondary side;

$L_{2\sigma}$ leakage inductance of the secondary winding

Interval t7−t8: Only the magnetizing current flows through the primary winding of the power transformer in this interval. This small magnetizing current is turned OFF by primary switches and thus zero current turn off is achieved. The current of the smoothing inductance LO is flowing through the freewheeling diode DO now.



(g)

(g) Operation in interval t7−t8

The smoothing inductance current ripple is

$$\Delta i_{Lo} = \frac{U_o}{L_o}\frac{T}{2}(1-d) \quad (12)$$

Where d= (t_{on}− T /2) /T/ 2 is duty cycle The output voltage can be determined as

$$U_o = \frac{\left(t_{ON}-\frac{T}{2}\right)}{\frac{T}{2}}\frac{U_1}{n} = d\frac{U_1}{n} \quad (13)$$

B. Snubber Design

Simplified design of the snubber parameters is demonstrated by applying or converting the previously derived equations. Value of the snubber capacitor is derived from (20), where the maximum permissible capacitor voltageUCc5is chosen

$$C_{C5} \approx \frac{\left(i_o+\frac{\Delta i_{Lo}}{2}\right)^2 (L'_{1\sigma}+L_{2\sigma})}{\left(U_{Cc5}-\frac{U_1}{n}\right)^2} \quad (14)$$

Entire energy of the leakage inductance is accumulated in the snubber capacitor at turn off of the secondary switch. The higher the leakage inductance of the power transformer referred to the secondary side

$L'_\sigma = L'_{1\sigma} + L_{2\sigma}$ the higher must be snubber capacitance, so that the capacitor voltageUCc5would not exceed maximum permissible value. Thus,

leakage inductance of the transformer should be as small as possible. Charging timetCc5ch of the snubber capacitor is calculated from (19). If the maximum discharging currentICc5dchis chosen, then value of the snubber inductor expressed from (6) is as follows:

$$L_{S5} = \frac{C_{C5}\left(U_{Cc5}-\frac{U_1}{n}\right)^2}{I^2_{Cc5dch}} \qquad (15)$$

The snubber capacitor discharging timetCc5dch is given by (4) and decay time tLS5dch of the snubber inductor can be calculated from (8).

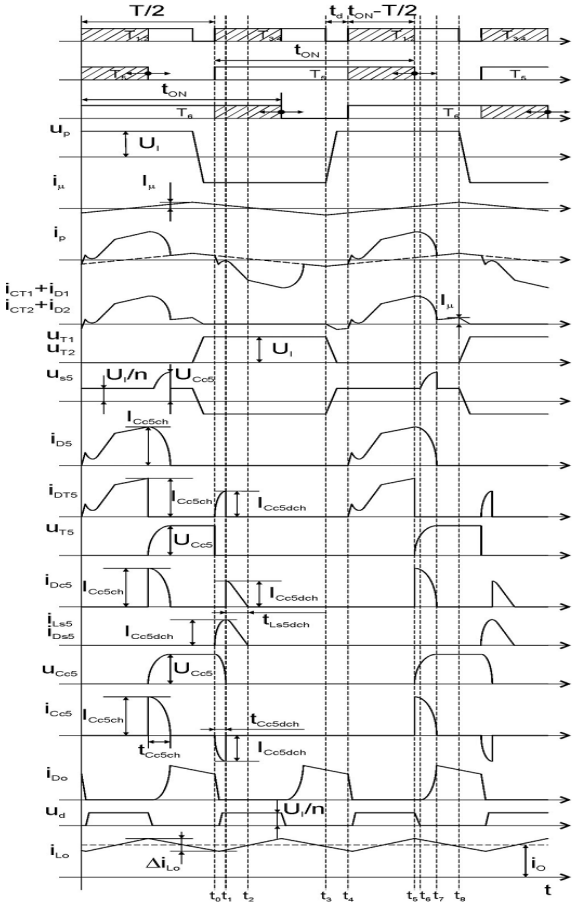


Fig. 5. Operation waveforms of the converter.

During discharging and decay times (tCc5dch+tLS5dch), the energy of the leakage inductance stored in the snubber capacitor is transferred to the load. According to the proposed control algorithm, there is enough time for discharging and decay of the snubber current during leakage inductance energy transfer—at least half of period. Therefore, low value of the discharging current can be chosen, which is one of the advantages of this way of control.

TABLE I
COMPONENTS IN ACONVERTER

T_1-T_4	IRG4PSC71UD
T_5,T_6	2xIRFP4568
D_5,D_6 D_{C5}, D_{S5}, D_{C6},	150EBU02
D_O	2x150EBU02
L_{S5}, L_{S6}	0.3 µH
C_{S5}, C_{S6}	220 nF
L_O	5.3 µH
C_O	100 µF

TABLE I I
PLANARTRANSFORMERPARAMETERS

Core	2xE64
Material	3C90
Turn´s ratio n = n_p/n_s	5:1
Primary winding resistance R_1	6.5 mΩ
Secondary winding resistance R_2	0.75 mΩ
Magnetizing inductance L_{1H}	706 µH
Leakage inductance referred to primary side L_6	625 nH
Weight	0.52 kg

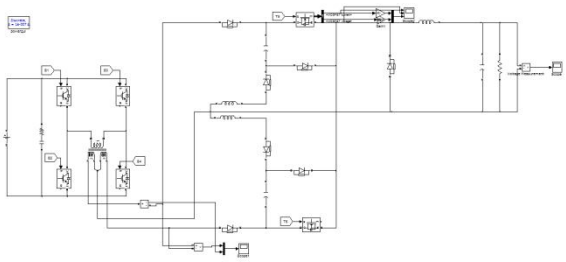


Fig. 6 Block diagram of simulation

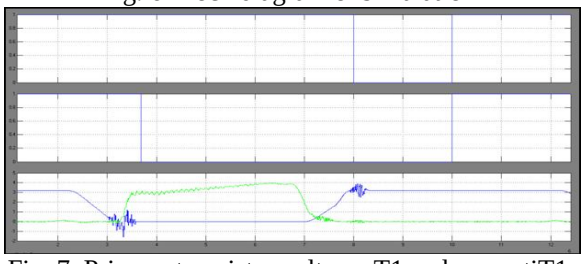


Fig. 7. Primary transistor voltageuT1 and currentiT1 at turn on and turn off and gate signals for secondaryuGST5 and primaryuGET1 transistors.

This small magnetizing current is later turned OFF by primary IGBTs and thus only negligible turn-off losses occur. At the turn on of the primary IGBTs, the primary current (transformer magnetizing current) discharges their output capacitances to zero. The rate of rise of the collector current is limited by the leakage inductance of transformer and thus zero voltage zero current turn on is ensured for primary IGBTs. Switching trajectory of the primary transistor is shown in Fig. 8.

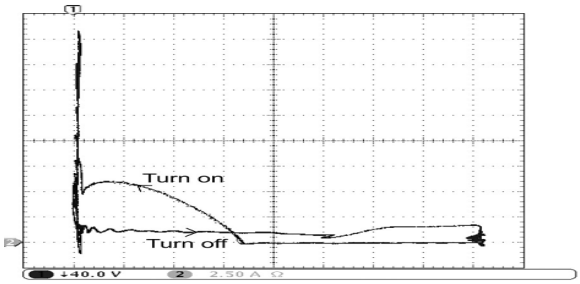


Fig. 8. Switching trajectory of the primary IGBT

It is evident that operating point of the primary transistor is moving in the low losses area. Primary voltage and current of power planar transformer are shown in Fig. 9.

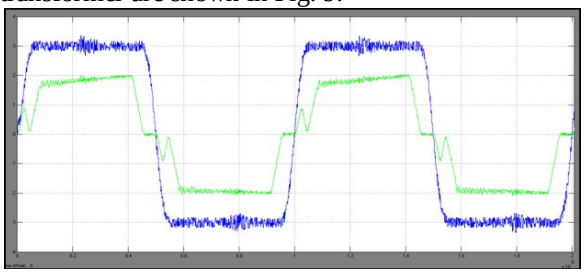


Fig. 9. Primary voltage uP and current iP of the transformer.

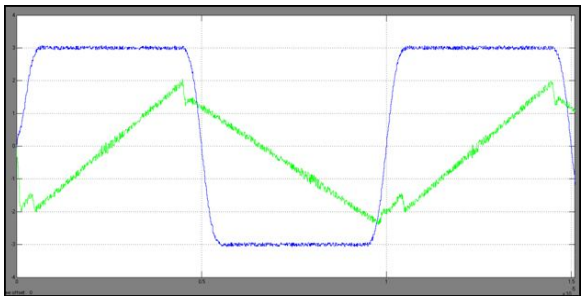


Fig. 10. Primary voltageuP and currentiP of the transformer at no-load.

Primary voltage up and primary current ip of the transformer Tr at no-load are shown in Fig. 10.

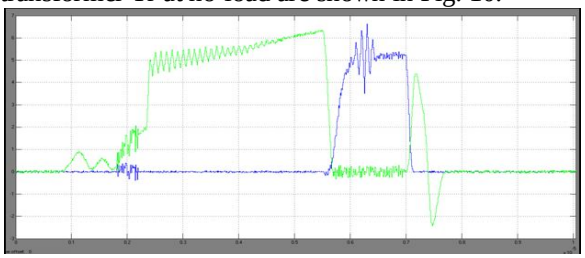


Fig. 11. Secondary transistor voltageuT5 and currentiDT5 at turn on and turn off

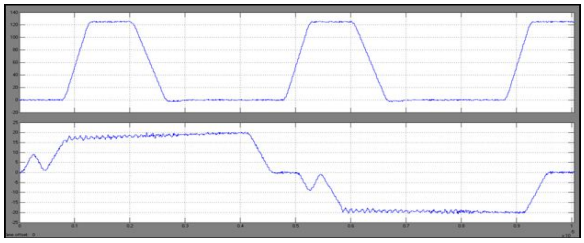


Fig. 12. Snubber capacitor voltageuCc5 and snubber capacitor currentiCc5 at charging and discharging

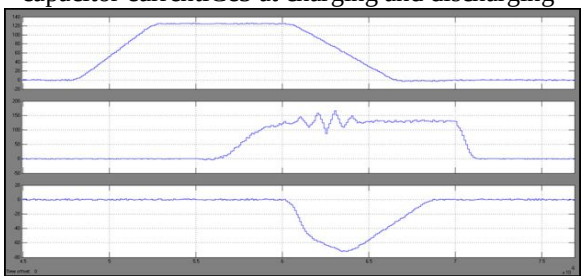


Fig. 13. Snubber capacitor voltageuCc5, secondary transistor voltageuDS5, and snubber inductor currentiLS5 at charging and discharging of the capacitor CC5

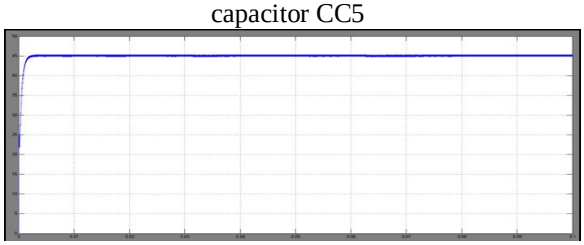


Fig. 14. Measured load characteristic of the converter

CONCLUSION

In this paper we are described about the topology of PWM dc–dc converter which is permits all switching devices to perform under soft switching by using a controlled rectifier and the turn-off snubber. In this paper the proposed converter with the soft switching and reduction of circulating currents is utilized for full-load range using a secondary-side turn-off snubber in combination with a controlled output rectifier and an appropriate control algorithm. Therefore according to the proper design, we can estimate the utilize magnetizing current of the power transformer for charging or discharging output capacitances of the IGBT switches which is to achieve the zero voltage turn on of the IGBTs. According to the zero current the IGBTs are turned OFF. Moreover, the snubber ensures zero current turn on and zero voltage turn off of the secondary switches. IGBTs in the full-bridge inverter operate at almost ideal switching conditions—zero voltage turn on and zero current turn off, which is the main advantage of the proposed converter.

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