

CONTROL OF RIPPLE ELIMINATORS TO IMPROVE THE POWER QUALITY OF DC SYSTEMS AND REDUCE THE USAGE OF ELECTROLYTIC CAPACITORS

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ABSTRACT- In this paper, a single-phase Pulse width modulation-controlled rectifier is proposed in this paper. The active control strategies can improve the power quality of dc systems, reduce voltage ripples, and, at the same time, reduce the usage of electrolytic capacitors. The concept of ripple eliminators is proposed and developed for future development, and the ratio of capacitance reduction is quantified. The main aim of this paper is to investigate how advanced control strategies could improve the performance of ripple eliminators. An advanced controller on the basis of the repetitive control is proposed for one possible implementation of ripple eliminators in the continuous current mode (CCM). By using the simulation results we can verify the effectiveness of the strategy with comparison to another ripple eliminator operated in the discontinuous current mode.

KEY WORDS: Instantaneous diversion of ripple currents, CCM, DCM, ripple eliminators, voltage ripples, repetitive control, reliability, electrolytic capacitors.

INTRODUCTION

In principle, this power quality issue in DC systems stems from energy fluctuation, which can come from sources and/or loads of systems. Four main approaches have been developed in the literature to reduce or compensate energy fluctuation so that the voltage ripples can be reduced and the power quality in DC systems can be improved. In such DC systems, ripple power is often not a major concern because a DC current is constant and there is not a problem of the phase differences between the currents and voltages. Therefore there are various applications such as wind power systems, rectifiers and inverters and hybrid electrical vehicles are most normally used for the DC voltages are not ideal but have a significant amount of harmonic components [3]. Because of the harmonic components in the voltages and the resulting ripple currents, ripple power has become a major power quality issue in DC systems.

Artificial neural networks are algorithms that can be used to perform nonlinear statistical modeling and provide a new alternative to logistic regression, the most commonly used method for

developing predictive models for dichotomous outcomes in medicine. During the charging mode of a battery, an external voltage with large ripples could lead to an immoderate chemical reaction. During the discharging mode, ripple currents drawn from a fuel cell can degrade the system efficiency significantly. Generally, current ripples should be maintained less than 10% of the rated current for batteries [8]. In order to reduce the ripple current and smooth the external voltage on batteries and fuel cells, bulky capacitors or ultra capacitors are often connected in parallel with them [9]. Large electrolytic capacitors are also often needed to level and smooth the DC-bus voltage of inverters and rectifiers [10].

Neural networks offer a number of advantages, including requiring less formal statistical training, ability to implicitly detect complex nonlinear relationships between dependent and independent variables, ability to detect all possible interactions between predictor variables, and the availability of multiple training algorithms. Compared to the conference version of this paper, the new contributions of this paper include 1) analyzing and revealing how active control strategies can help reduce voltage ripples and reduce total capacitance, which paves a way to design high performance controllers for different types of ripple eliminators; 2) quantifying the level of capacitance reduction, which is independent from applications and topologies; 3) optimizing the controller for ripple eliminators in which only one instead of two repetitive controllers are now required without affecting the system performance; 4) verifying the performance of the active control strategies.

The analysis in these papers is based on the fact that decreased pulsating input power leads to decreased ripple power and capacitor volume on the DC bus, which can be achieved by controlling the input current.

The main focus of this paper is to investigate how advanced control strategies could improve the performance of shunt ripple eliminators for DC systems, rather than optimizing the system

performance through topological design. It is preferred to operating the shunt ripple eliminator in the continuous current mode (CCM) rather than in the discontinuous current mode (DCM) because the current tracking is instantaneous in CCM but is in the average sense in DCM. Because the ripple current is diverted instantaneously in CCM, the voltage ripples can be reduced considerably. It is a bidirectional boost converter that is able to divert the ripple current instantaneously.

II. ANALYSIS OF RIPPLE ENERGY AND RIPPLE VOLTAGE

In order to facilitate the analysis in this paper, a single-phase H-bridge PWM-controlled rectifier as shown in Figure 1 is used as an example, with all the components assumed to be ideal to simplify the analysis in the sequel.

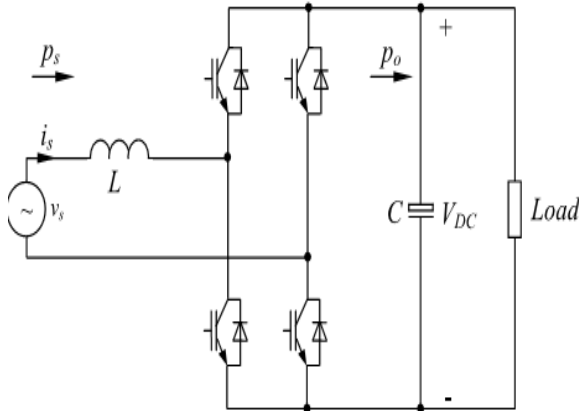


Fig 1. Single-phase H-bridge PWM-controlled rectifier.

If the input current of the rectifier is regulated to be sinusoidal as $i_s = \sqrt{2}I_s \sin(\omega t)$ and in phase with the input voltage $v_s = \sqrt{2}V_s \sin(\omega t)$, then the input power is

$$p_s = v_s i_s = V_s I_s - V_s I_s \cos(2\omega t) \quad (1)$$

where V_s and I_s are the RMS values of the input voltage and current, respectively, and ω is the angular line frequency.

RIPPLE ELIMINATORS AND THE LEVEL OF CAPACITANCE REDUCTION

In order to break the deadlock between minimizing the required capacitors and reducing voltage ripples, another design degree of freedom, called the ripple eliminator [9], can be introduced to replace the bulky DC-bus capacitor, as shown in Figure 2.

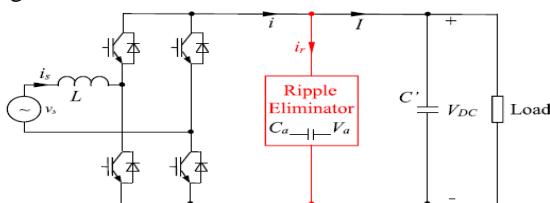


Fig.2.The concept of ripple eliminators.

Since the ripple eliminator is operated to divert the ripple energy on the DC bus to the auxiliary capacitor, there is no need to use a large electrolytic capacitor on the DC bus and the ripple energy on the auxiliary capacitor should be the same as the DC-bus ripple energy in the ideal case.

$$C_a \approx \frac{E_r}{\Delta V_a V_{a0}} \quad (3)$$

where ΔV_a and V_{a0} are the peak-peak and average voltages of the auxiliary capacitor. Note that the ripple energy E_r is determined by the DC bus and not affected by the added ripple eliminator. Note also that the auxiliary capacitor is designed to allow large voltage ripples. Assume the ripple voltage ratio of the auxiliary capacitor is

$$r_a = \frac{\Delta V_a}{V_{a0}} \quad (4)$$

Then (4) can be re-written as

$$C_a \approx \frac{E_r}{r_a V_{a0}^2} \quad (5)$$

It is clear that for the same ripple ratio r_a , the capacitance is in inverse proportion to the square of the voltage across it, which means the auxiliary capacitance can be significantly reduced via increasing its operating voltage.

If the same ripple energy E_r needs to be taken care of by a DC-bus capacitor C , as shown in Figure 2, then, according to (3), the voltage ripple ratio r of the DC bus is about

$$r \approx \frac{E_r}{C V_{DC0}^2} \quad (6)$$

This means the auxiliary capacitor needed can be reduced to

$$C_a \approx \frac{r}{r_a} \left(\frac{V_{DC0}}{V_{a0}} \right)^2 C \quad (7)$$

By a factor of

$$R_d = \frac{r}{r_a} \left(\frac{V_{DC0}}{V_{a0}} \right)^2 = \frac{\Delta V_a V_{a0}}{\Delta V_{DC} V_{DC0}} \quad (8)$$

The capacitance C_a can be reduced by 1) allowing the voltage ripple ratio higher than that of the original DC bus, 2) adopting an operating voltage V_{a0} higher than V_{DC0} for C_a .

It sets the basic guidelines for designing different ripple eliminators. Some other guidelines include: 1) a ripple eliminator needs to be able to provide bi-directional current path so that the ripple current; 2) the remaining level of DC-bus voltage ripples is determined by the performance of the ripple eliminator so the ripple eliminator needs to be controlled properly; 3) The hold-up time requirement, voltage stress and current stress should be considered to choose suitable capacitors.

THE RIPPLE ELIMINATOR UNDER INVESTIGATION

Operation principles of the ripple eliminator

In this paper, a practical implementation of the ripple eliminator concept to be studied is shown

in the dashed box of Figure 3, which is actually a bi-directional boost-buck converter.

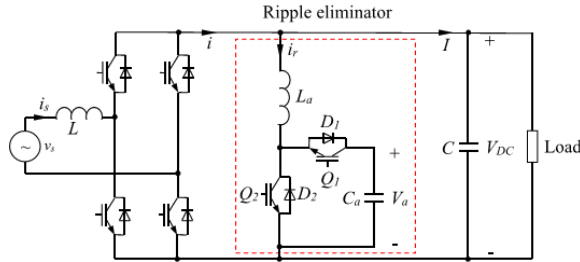


Fig 3. The ripple eliminator under investigation.

In order to track the ripple current, switches Q1 and Q2 can be controlled in two different switching modes. One is only to control Q2 (Q1, resp.) in the positive (negative, resp.) half cycle of the ripple current, which corresponds to the charging (discharging) mode. In the charging mode, Q2 is controlled by a PWM signal and Q1 is always OFF, which provides the path for the positive half cycle of the ripple current i_r , and hence, the ripple eliminator is operated as a boost converter. In the discharging mode, Q2 is always OFF and Q1 is controlled by a PWM signal, which provides the path for the negative half cycle of the ripple current i_r , and the circuit is operated as a buck converter. Therefore, the direction of the current owing through the auxiliary inductor can only be negative or positive in one switching period.

Another switching mode is to control the two switches complementarily. That means switches Q1 and Q2 are controlled by two inverse PWM signals to track the ripple current and the voltage across the auxiliary inductor can be V_{DC} and $V_{DC} - V_a$ depending on the ON-OFF combinations of these two switches. In one PWM period, if Q1 is ON, Q2 is controlled by an inverse signal to keep OFF and vice versa. In this paper, in order to fully use the ripple eliminator under different working conditions, Q1 and Q2 are operated complementarily to track the ripple current.

Selection of the auxiliary inductor

As two switches Q1 and Q2 are operated complementarily, the ON time of Q2 is $d_r T_r$ and the ON time of Q1 is T_r in one PWM period. Since the PWM frequency is much higher than the line frequency, it can be assumed that the current increased (to withstand the positive voltage VDC) and decreased (to withstand the negative voltage) in these two modes are the same in the steady state. In other words, the current ripple $4i_r$ is

$$\Delta i_r = \frac{V_{dc}}{L_a} d_r T_r = -\frac{V_{DC}-V_a}{L_a} (1-d_r) T_r \quad (9)$$

Therefore, the duty cycle d_r can be obtained as

$$d_r = 1 - \frac{V_{DC}}{V_a} \quad (10)$$

The substitution of (9) into (8) leads to

$$\frac{L_a \Delta i_r}{V_{dc}} = \left(1 - \frac{V_{dc}}{V_a}\right) T_r \quad (11)$$

which can be re-written as

$$f_r L_a \Delta i_r = V_{dc} \left(1 - \frac{V_{dc}}{V_a}\right) \quad (12)$$

The product of the switching frequency f_r , the inductance L_a and the current ripple $4i_r$ is a constant, which is determined by the DC-bus voltage and the auxiliary voltage. The auxiliary inductor current mainly includes the current ripple i_r and the ripple current to be injected into the DC-bus. The high frequency part of i_r , which is $1i_r$, can be large in order to reduce the inductance of L_a . In order to ensure the inductor is operated in the critical continuous current mode, the amplitude of Δi_r is designed to satisfy

$$\Delta i_r \leq 2I_{rm} \quad (13)$$

where I_{rm} is the peak value of i_r . Considering (12), the auxiliary inductance should be selected to satisfy

$$L_a \geq \frac{\left(1 - \frac{V_{dc}}{V_a}\right) V_{dc}}{2I_{rm} f_r} \quad (14)$$

The rising rate of the auxiliary inductor current should be greater than the maximum rising rate of the reference ripple current which appears at the zero-crossing point. If the reference ripple current is expressed as

$$i_r = I_{rm} \sin(2\omega t) \quad (15)$$

then the maximum rising rate of i_r can be obtained as

$$\left. \frac{di_r}{dt} \right|_{t=0} = 2\omega I_{rm} = 4\pi f I_{rm} \quad (16)$$

Accordingly, there exist

$$\frac{V_{DC}}{L_a} \geq 4\pi f I_{rm} \quad (17)$$

And

$$\frac{V_a - V_{DC}}{L_a} \geq 4\pi f I_{rm} \quad (18)$$

Combining the above two equations, then

$$L_a \leq \min\left(\frac{V_{DC}}{4\pi f I_{rm}}, \frac{V_a - V_{DC}}{4\pi f I_{rm}}\right) \quad (19)$$

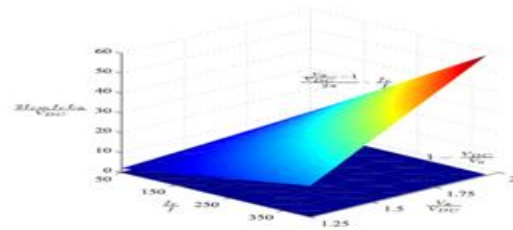


Fig.4. Selection of $2I_{rm} f_r L_a$ VDC V between the two surfaces.

CONTROL OF THE RIPPLE ELIMINATOR

Formulation of the control problem

The DC voltage ripple is caused by the pulsating input energy. After the ripple eliminator is introduced to divert the ripple current from the capacitor C, the DC-bus voltage then becomes ripple free, apart from switching ripples, and equal to the

DC-bus voltage. Hence, the current to be diverted should be

$$i_r = -\frac{V_s I_s}{V_{DC0}} \cos(2\omega t) \quad (20)$$

which is a second-order harmonic current.

The control objective of the ripple eliminator is then to instantaneously divert i_r . The control problem is to instantaneously track the ripple current i_r that corresponds to the ripple power via controlling Q1 and Q2.

In this paper, the CCM operation is chosen because of its high performance for current tracking. The ripple current tracking can be achieved in two steps: 1) to generate a reference ripple current and 2) to track the reference ripple current. Moreover, in order to make sure that the current tracking can be achieved properly, the voltage across the auxiliary capacitor C_a should be regulated as well. The proposed overall control strategy is shown in Fig.5, which is explained in detail in the following subsections.

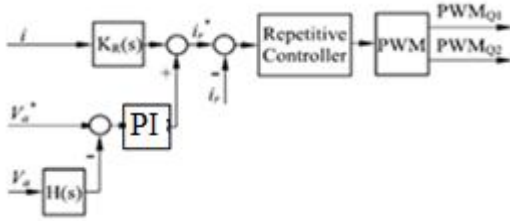


Fig.5 Control strategy for the ripple eliminator.

Regulation of the auxiliary capacitor voltage

The operation of the ripple eliminator relies on a properly regulated the voltage across the auxiliary capacitor, which is designed to allow a significant amount of ripples. For the purpose of maintaining the average DC component at a certain value, a low-pass filter can be adopted to remove ripples.

$$H(s) = \frac{1-e^{-\tau s/2}}{\tau s/2} \quad (21)$$

The following low-pass filter in which is chosen as the system fundamental period, is used. Once the average voltage is obtained, it can be easily regulated at a given value V a by using a PI controller, as shown in Figure 6, via charging or discharging the ripple eliminator.

Generation of the reference ripple current i_r^*

The second-order harmonic current of the current i between the rectifier and the ripple eliminator can be extracted by using the following resonant filter tuned at the second harmonic frequency. If the harmonic current has components at other frequencies, then $K_R(s)$ can be designed to include the corresponding term. For example, if there is a 3rd-order harmonic current, then $K_R(s)$ can include a term with $h D 3$. The extracted current can be added to the output of the PI controller that

regulates the auxiliary capacitor voltage to form the reference ripple current.

$$K_R(s) = \frac{K_h 2\xi h \omega s}{s^2 + 2\xi h \omega s + (h\omega)^2} \quad (22)$$

Design of a current controller to track the second-order ripple current

The control problem is essentially a current tracking problem. Since the reference ripple current is periodic, the repetitive control strategy can be adopted to achieve excellent tracking performance with a fed switching frequency, as shown in Figure 6.

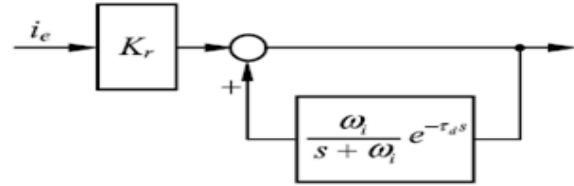


Fig.6. The repetitive controller.

A repetitive controller contains an internal model, which is a local positive feedback loop involving a delay term and a low-pass filter, as shown in Figure 7. In this paper, since the problem is a current tracking problem, the proportional controller K_r cascaded with the internal model obtained with the H1 control strategy, as shown in Figure 7, is adopted.

Based on the analysis in [30] and [33], d is selected as

$$\tau_d = \frac{\tau}{2} - \frac{1}{\omega_i} = 0.0099s \quad (23)$$

The proportional gain can be determined by following the procedures of H1 control design proposed or simply by tuning with trial-and-error.

System parameters

In order to verify the proposed control method, a test rig that consists of a 1:1 kW single-phase PWM-controlled rectifier and three kinds of ripple eliminators was built. The system parameters are summarized in Table 1.

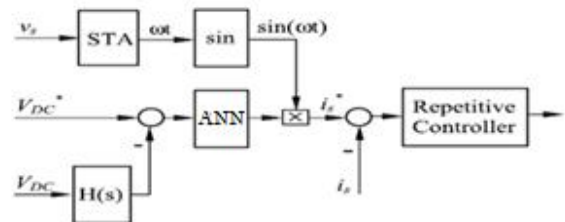


Fig.7. Controller for a single-phase PWM-controlled rectifier.

Control of the single-phase PWM-controlled rectifier

The PWM rectifier is adopted as an example for generating voltage/current ripples in a DC system. It is controlled to draw a clean sinusoidal current from the source that is in phase with the voltage source. This can be achieved with the controller

shown in Figure 8, which mainly consists of three parts: 1) a synchronization unit to generate a clean sinusoidal current signal that is in phase with the source so that the reactive power drawn from the supply is controlled to be zero; 2) a PI voltage controller that maintains the voltage VDC according to the DC-bus reference voltage VDC to generate the right amplitude for the current reference; and 3) a current controller to track the reference current that is formed according to the PI voltage controller and the synchronization signal.

Validation

Without the ripple eliminator

The input current was well regulated to be in phase with the source voltage to achieve the unity power factor. However, the ripple of the VDC is around 90 V, which is often not acceptable in practice.

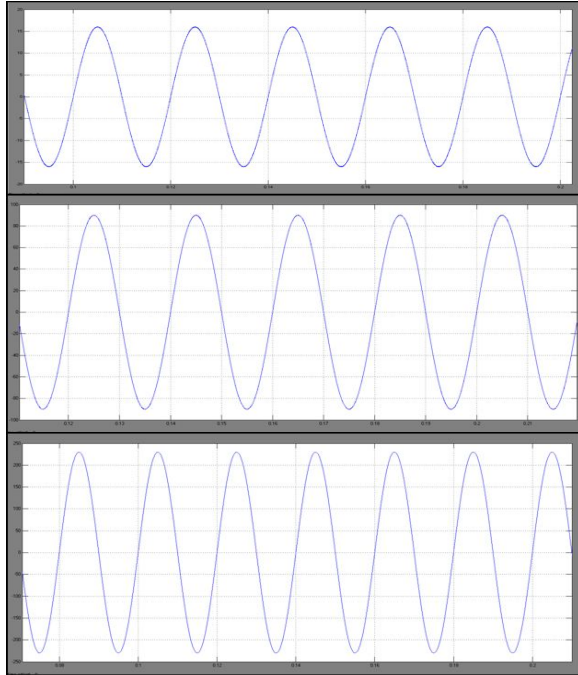


Fig.12 with out ripple eliminator

With the ripple eliminator activated

Figure 10 shows the results with the ripple eliminator activated. In order to investigate how the voltage V_a affects the reduction of the voltage ripple, different levels of the V_a at 500 V, 600 V and 700 V were tested. Generally, it can be seen that the DC-bus voltage ripple was significantly reduced for all these three voltages. The performance is improved when the auxiliary capacitor voltage is increased because the inductor current tracking performance is improved when the auxiliary capacitor voltage

increases.

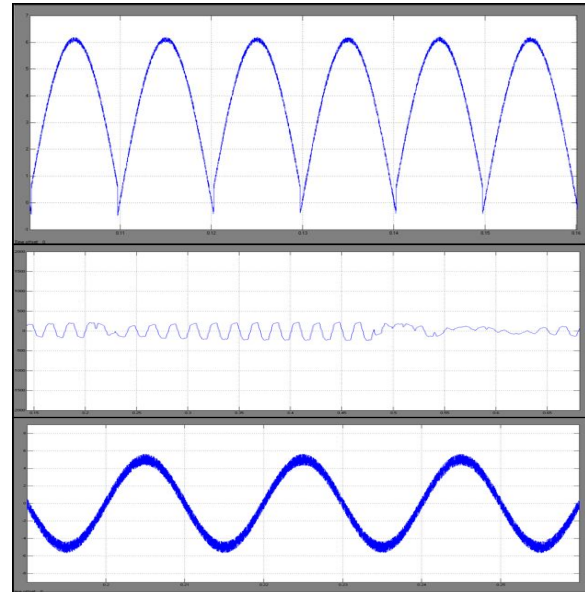


Fig.13. With ripple eliminator at 500v

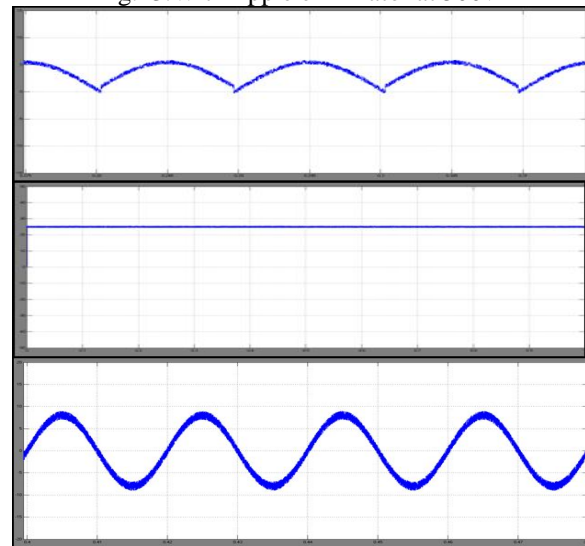
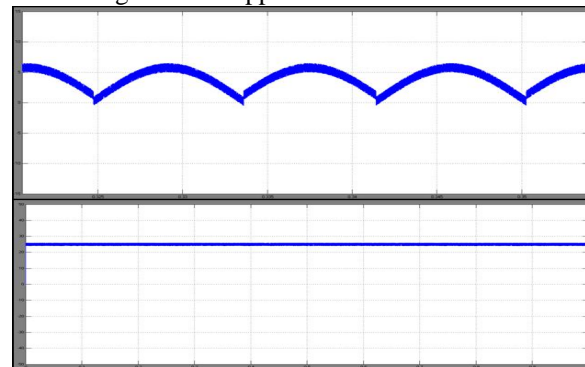


Fig.14. With ripple eliminator at 600V



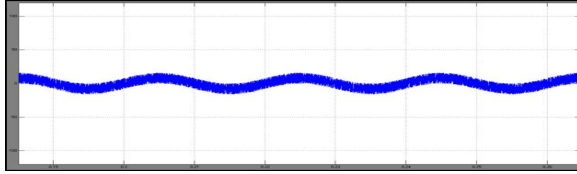


Fig.15. With ripple eliminator at 700v

Dynamic performance

The dynamic performance of the ripple eliminator was tested. The voltage ripple was almost removed from the DC-bus voltage after the eliminator was activated for about seven line cycles.

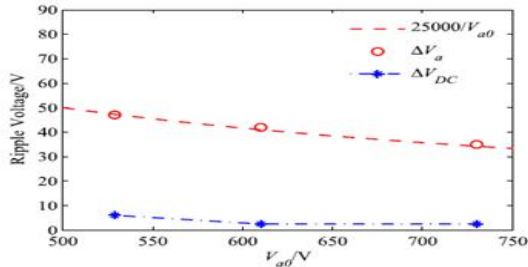


Fig.16 Voltage ripples on the DC bus (1VDC) and the capacitor Ca (1Va) of the proposed ripple eliminator tested over a wide range of Va0.

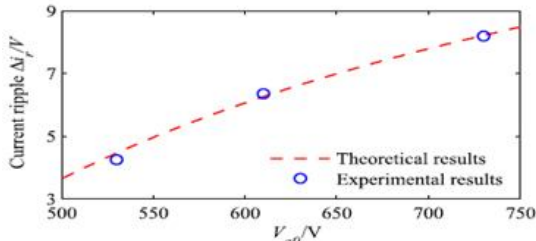


Fig.17. Current ripples Iir on the inductor La over a wide range of Va0.

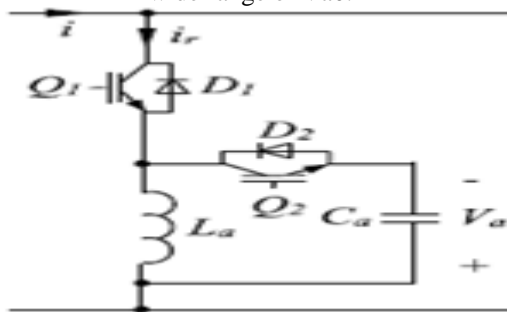


Fig.18. The DCM ripple eliminator studied (a) topology;

Comparison with the DCM ripple eliminator

This makes the ripple eliminator either a buck or a boost converter and hence, both $V_a < V_{DC}$ and $V_a > V_{DC}$ can be achieved. The inductor L_a is changed to 0.55 mH so that the eliminator can be operated in DCM. The other parameters of the system are the same as given in Table 1.

TABLE.1 SYSTEM PARAMETERS

Parameters	Values
AC voltage (RMS)	230 V
System fundamental frequency	50 Hz
Switching frequency	10 kHz
Inductor L	2.2 mH
Inductor L_a	2.2 mH
Capacitor C	110 μ F
Auxiliary capacitor C_a	165 μ F
Voltage V_{DC}	400 V

CONCLUSION

The concept of ripple eliminators has been further developed to improve the power quality and reduce the voltage ripples in DC systems and, at the same time, reduce the capacitance needed and the usage of electrolytic capacitors. This paper has the following unique contributions: 1) It has been revealed that the capability of instantly diverting the ripple current away from the DC bus is the key to improve the performance. ripple eliminators that can be operated in CCM to instantaneously divert ripple currents are preferred; 2) the repetitive control strategy is proposed to control one exemplar ripple eliminator, with the ripple energy provided by a single-phase PWM-controlled rectifier. Simulation results have demonstrated that the proposed strategy is valid and offers several times of performance improvement with comparison to a DCM ripple eliminator reported.

REFERENCES

[1] Q.-C. Zhong, W.-L. Ming, X. Cao, and M. Krstic, "Reduction of DC-bus voltage ripples and capacitors for single-phase PWM-controlled rectifiers," in Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc. (IECON), Oct. 2012, pp. 708713.

[2] A. A. Hamad, H. E. Farag, and E. F. El-Saadany, "A novel multiagent control scheme for voltage regulation in DC distribution systems," IEEE Trans. Sustainable Energy, vol. 6, no. 2, pp. 534545, Apr. 2015.

[3] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," IEEE Trans. Power Electron., vol. 31, no. 7, pp. 47784794, Jul. 2016.

[4] Y. Du, D. D.-C. Lu, G. M. L. Chu, and W. Xiao, "Closed-form solution of time-varying model and its applications for output current harmonics in two-stage PV inverter," IEEE Trans. Sustainable Energy, vol. 6, no. 1, pp. 142150, Jan. 2015.

[5] B. Karanayil, V. G. Agelidis, and J. Pou, "Performance evaluation of three-phase grid-connected photovoltaic inverters using electrolytic or polypropylene Im capacitors," IEEE Trans. Sustainable Energy, vol. 5, no. 4, pp. 12971306, Oct. 2014.

- [6] Y. Hu, W. Cao, S. J. Finney, W. Xiao, F. Zhang, and S. F. McLoone, "New modular structure DCDC converter without electrolytic capacitors for renewable energy applications," *IEEE Trans. Sustainable Energy*, vol. 5, no. 4, pp. 1184-1192, Oct. 2014.
- [7] C. Liu and J.-S. Lai, "Low frequency current ripple reduction technique with active control in a fuel cell power system with inverter load," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1429-1436, Jul. 2007.
- [8] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems," *IEEE Trans. Veh. Technol.*, vol. 61, no. 7, pp. 2950-2964, Sep. 2012.
- [9] W. Choi, J.W. Howze, and P. Enjeti, "Development of an equivalent circuit model of a fuel cell to evaluate the effects of inverter ripple current," *J. Power Sour.*, vol. 158, no. 2, pp. 1324-1332, Aug. 2006.
- [10] R. Wang et al., "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430-1443, May 2011.



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