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REDUCED NUMBER OF POWER ELECTRONIC COMPONENTS WITH THREE-PHASE MULTILEVEL INVERTER

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ABSTRACT-In this paper a new configuration of a three-phase five-level multilevel voltage-source inverter is proposed. This paper suggests a novel topology for a three phase five-level multilevel inverter. The number of switching devices, insulated-gate driver circuits, and installation area and cost are significantly reduced. This paper presents a new topology for a 3-ϕ, three step multilevel inverter (MLI) with Common Mode Voltage (CMV) elimination. Compared to existing inverters (particularly in higher levels) this topology requires fewer components and requires fewer carrier signals and gate drives. The proposed topology constitutes the conventional three-phase two-level bridge with three bidirectional switches. A multilevel dc link using fixed dc voltage supply and cascaded half-bridge is connected in such a way that the proposed inverter outputs the required output voltage levels. If we increasing the number of voltage level with fewer number of power electronic components, the structure of the proposed inverter is extended and different methods to determine the magnitudes of utilized dc voltage supplies are suggested.By using the simulation results we can ensure that the feasibility of the configuration and the compatibility of the modulation technique.

Index Terms—Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter.

INTRODUCTION

Multilevel inverters have been widely accepted for high-power high-voltage applications. Their performance is highly superior to that of conventional two-level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages. Multilevel inverters consist of a group of switching devices and dc voltage supplies, the output of which produces voltages with stepped waveforms. Multilevel technology has started with the three-level converter followed by numerous multilevel converter topologies. Different topologies and wide variety of control methods have been developed in the recent literature [1]–[3].

The most common multilevel inverter configurations are neutral point clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge (CHB). The deviating voltage of neutral-point voltage in NPC, the unbalanced voltage in the dc link of FC, and the large number of separated dc supplies in CHB are considered the main drawbacks of these topologies [4], [5].

In the asymmetrical configurations, the magnitudes of dc voltage supplies are unequal. These topologies reduce the cost and size of the inverter and improve the reliability since minimum number of power electronic components, capacitors, and dc supplies are used.

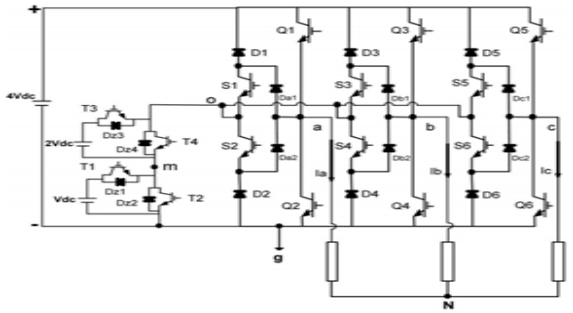
The hybrid multistage converters consist of different multilevel configurations with unequal dc voltage supplies. With such converters, different modulation strategies and power electronic components technologies are needed [4]. For the purpose of improving the performance of the conventional single- and three-phase inverters, different topologies employing different types of bidirectional switches have been suggested. Comparing to the unidirectional one, bidirectional switch is able to conduct the current and withstanding the voltage in both directions.

Bidirectional switches with an appropriate control technique can improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the high number of voltage level with an effective application of a fundamental frequency staircase modulation technique.

MODELLING OF PROPOSED THEORY

Proposed topology:

Fig. 1(a) and (b) shows the typical configuration of the proposed three-phase five-level multilevel inverter.



(a)

Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the

conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint. A multilevel dc link built by a single dc voltage supply with fixed magnitude of 4Vdcand CHB having two unequal dc voltage supplies of Vdc and 2Vdc are connected to (+,–,o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used.

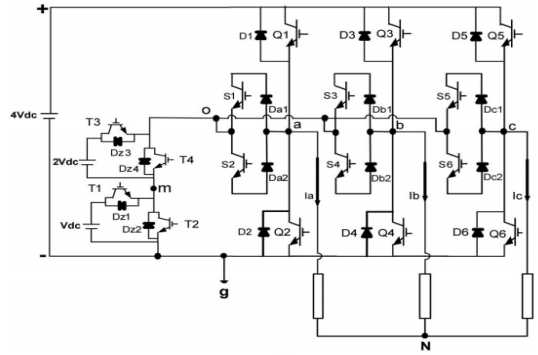


Fig. 1. Circuit diagram of the proposed three-phase five-level multilevel inverter

The peak voltage rating of the switches of the conventional two level bridge (Q1–Q6) is 4Vdcwhereas the bidirectional switches(S1–S6) have a peak voltage rating of 3Vdc.InCHBcells,thepeak voltage rating of second cell switches (T3 and T4) is 2Vdcwhile the peak voltage rating of T1 and T2 in the first cell is Vdc. By considering phase, the operating status of the switches and the inverter line-to-ground voltage Vag are given in Table I.

TABLE I
Switching State Sa and Inverter Line-to-Ground Voltage Va

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
4	on	off	off	off	on	off	on	off	+4Vdc
3	off	on	on	off	on	off	on	off	+3Vdc
2	off	on	on	off	off	on	on	off	+2Vdc
1	off	on	on	off	on	off	off	on	+Vdc
0	off	off	off	on	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages Vag, Vbg, and Vcg in terms of switching states Sa, Sb, and Scas

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} (1)$$

Where N=5 is the maximum number of voltage levels. The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity.

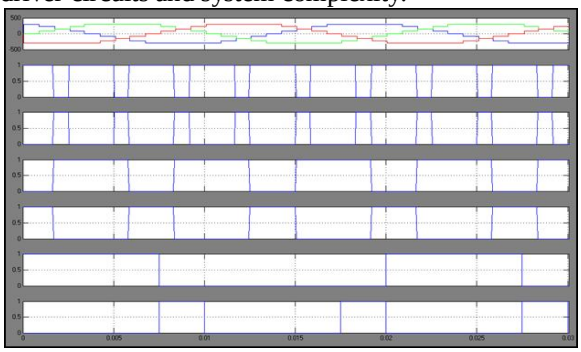


Fig. 2. Simulated waveforms ofVab,Vbc,andVca with corresponding switching gate signals fo the proposed inverter at fundamental frequency f=50 Hz.

The inverter line-to-line voltage waveforms Vab, Vbc, and Vca with corresponding switching gate signals are depicted in Fig. 2whereVab,Vbc, and Vca are related to Vag, Vbg, and Vcg.

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} (2)$$

The inverter line-to-neutral voltages VaN, VbN, and VcN may be expressed as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} (3)$$

It is useful to recognize that the inverter voltages at terminals a, b, and c with respect to
the id point(o)are given by

$$\begin{bmatrix} V_{a0} \\ V_{b0} \\ V_{c0} \end{bmatrix} = \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} - \begin{bmatrix} V_{og} \\ V_{og} \\ V_{og} \end{bmatrix} (4)$$

whereVogis the voltage at midpoint(o)with respect to groun (g). Vogroutinely fluctuates among three different voltage valuesVdc,2Vdc, and 3Vdcas follows

$$V_{og} = \begin{cases} V_{dc}, & if S_a + S_b + S_c \leq 5 \\ 2V_{dc} if S_a + S_b + S_c = 6 \\ 3V_{dc} if S_a + S_b + S_c \geq 7 \end{cases} (5)$$

The simulated voltage waveforms ofVag,Vog,Vao, and VaN based on (1)–(5) are shown in Fig. 3

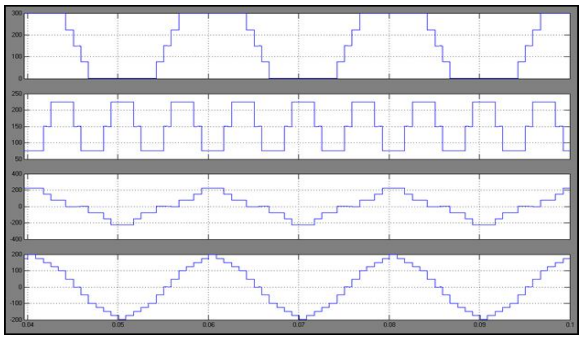


Fig. 3. Simulated waveforms of Vag, Vog, Vao, and VaN for the proposed inverter f=50 Hz.

TABLE I I
Switching states sequence of the proposed inverter with in one cycle

Sa Sb Sc	Period T [s]	ON switches Leg *a*	ON switches Leg *b*	ON switches Leg *c*	ON switches cascaded half-bridge	*Vag* [V]	*Vbg* [V]	*Vcg* [V]
400	t1	Q1	Q4	Q6	T1,T4	*4Vdc*	0	0
410	t2	Q1	S3, S4	Q6	T1,T4	*4Vdc*	*Vdc*	0
420	t3	Q1	S3, S4	Q6	T2,T3	*4Vdc*	*2Vdc*	0
430	t4	Q1	S3, S4	Q6	T1,T3	*4Vdc*	*3Vdc*	0
440	t5	Q1	Q3	Q6	T1,T3	*4Vdc*	*4Vdc*	0
340	t6	S1, S2	Q3	Q6	T1,T3	*3Vdc*	*4Vdc*	0
240	t7	S1, S2	Q3	Q6	T2,T3	*2Vdc*	*4Vdc*	0
140	t8	S1, S2	Q3	Q6	T1,T4	*Vdc*	*4Vdc*	0
040	t9	Q2	Q3	Q6	T1,T4	0	*4Vdc*	0
041	t10	Q2	Q3	S5, S6	T1,T4	0	*4Vdc*	*Vdc*
042	t11	Q2	Q3	S5, S6	T2,T3	0	*4Vdc*	*2Vdc*
043	t12	Q2	Q3	S5, S6	T1,T3	0	*4Vdc*	*3Vdc*
044	t13	Q2	Q3	Q5	T1,T3	0	*4Vdc*	*4Vdc*
034	t14	Q2	S3, S4	Q5	T1,T3	0	*3Vdc*	*4Vdc*
024	t15	Q2	S3, S4	Q5	T2,T3	0	*2Vdc*	*4Vdc*
014	t16	Q2	S3, S4	Q5	T1,T4	0	*Vdc*	*4Vdc*
004	t17	Q2	Q4	Q5	T1,T4	0	0	*4Vdc*
104	t18	S1, S2	Q4	Q5	T1,T4	*Vdc*	0	*4Vdc*
204	t19	S1, S2	Q4	Q5	T2,T3	*2Vdc*	0	*4Vdc*
304	t20	S1, S2	Q4	Q5	T1,T3	*3Vdc*	0	*4Vdc*
404	t21	Q1	Q4	Q5	T1,T3	*4Vdc*	0	*4Vdc*
403	t22	Q1	Q4	S5, S6	T1,T3	*4Vdc*	0	*3Vdc*
402	t23	Q1	Q4	S5, S6	T2,T3	*4Vdc*	0	*2Vdc*
401	t24	Q1	Q4	S5, S6	T1,T4	*4Vdc*	0	*Vdc*

$$V_q = \frac{4V_{dc}}{3(N-1)}(2S_a - S_b - S_c) \quad (6)$$

$$V_d = \frac{4V_{dc}}{\sqrt{3}(N-1)}(S_c - S_b) \quad (7)$$

$$V = V_q - jV_d \quad (8)$$

For all switching states presented in Table II, Fig. 4 show the space vector diagram for the proposed topology.

Switching algorithm

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms.

An alternative method is proposed to generate the inverter's switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of Sa, Sb, and Sc. The basis of the proposed method can be explained as following: For a given value of modulation index Ma and within a full cycle of the operation of the proposed inverter, the switching states Sa, Sb, and Scare determined instantaneously. The on-time calculations of Sa, Sb, and Sc directly depend on the instantaneous values of the inverter line-to-ground voltages. It is well known that the reference values of Vag, Vbg, and Vcg are normally given by

$$\begin{bmatrix} V_{ag-ref} \\ V_{bg-ref} \\ V_{cg-ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(\omega t) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{dc}}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (9)$$

Where wt is the electrical angle. Or

$$\begin{bmatrix} V_{ag-ref} \\ V_{bg-ref} \\ V_{cg-ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(\omega t) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \cos\left(\omega t - \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{dc}}{2} * \left[1 - \frac{M_a}{6}\cos(3\omega t)\right] \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} (10)$$

From (10), it can be noticed that the third harmonic component is added to the three-line-to-ground voltages. The third harmonic injection may increase the inverter fundamental voltage without causing over modulation. As a result, Ma can reach to 1.15 and Sa, Sb, and Sc can be simply determined by integrating the reference line-to-ground voltages as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = integer\left(\frac{N-1}{4V_{dc}} * \begin{bmatrix} V_{ag-ref} \\ V_{bg-ref} \\ V_{cg-ref} \end{bmatrix}\right) (11)$$

Comparison of the proposed modulation method with the staircase modulation with the selective harmonic method shows that the proposed modulation features less time.

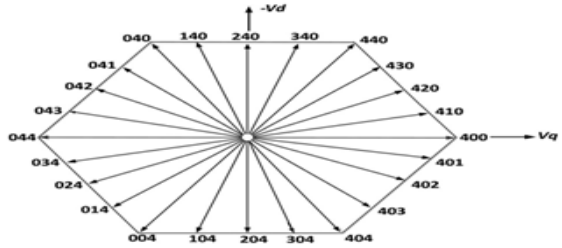


Fig. 4. Switching states vectors of the proposed inverter ind–q reference frame.

The inverter's operating switching states Sa, Sb, and Sc and corresponding switching gate signals based on the proposed modulation method are shown in Fig. 5.

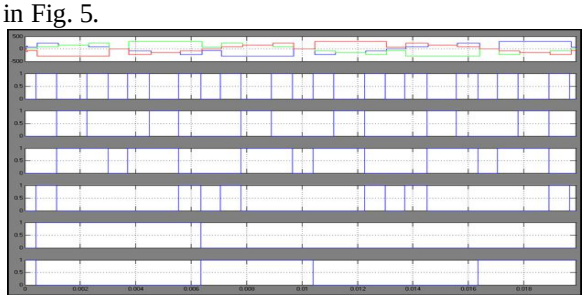


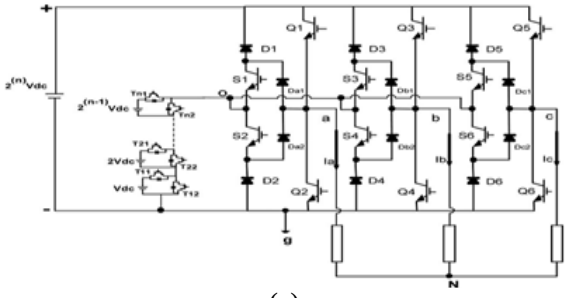
Fig. 5. Inverter's operating switching states Sa, Sb and Sc with corresponding witching gate signals based on the proposed modulation method.

TABLE III
SWITCHING STATES a1AND INVERTERLINE - TO-GROUND VOLTAGE Vag at Ma <0.9 (LEG a)

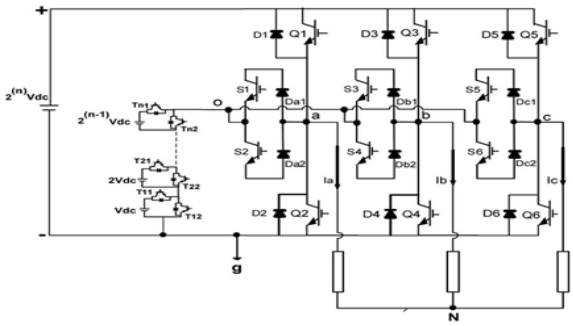
Sa1	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
2	on	off	off	off	off	on	on	off	+4Vdc
1	off	on	on	off	off	on	on	off	+2Vdc
0	off	off	off	on	off	on	on	off	0

Extended structure

It is noticeable that there is possibility to reach an output voltage with higher number of steps in the proposed multilevel inverter by extending the CHB circuit. Such extending can be done by adding more half-bridge cells connected in series as shown in Fig. 7(a) and (b).



(a)



(b)

Fig. 7. Circuit diagram of the proposed three-phase N-level multilevel inverter (third method)

In order to achieve the desired number of voltage levels, three methods can be followed to determine the magnitudes of utilized dc voltage supplies. 1) All cells have an equal dc supply in magnitude.

$$V_{dc1} = V_{dc2} = \cdots . = V_{dcn} = V_{dc} (12)$$

Then, the magnitude of fixed dc supply can be chosen as

$$V_{fix} = (N-1)V_{dc} = (1+n)V_{dc} (13)$$

Where n is the number of utilized cells. The maximum number

Of voltage steps is related to the number of utilized cells by

$$N = n + 2 (14)$$

The number of operation modes that makes the switching states sequence achieves the required output voltage waveform. Fig. 6(a) and (b) shows the inverter line-to-line voltage waveforms at five

different modulation indices including the over modulation operation Ma=0.8, 0.9, 1.05, 1.15, and 1.3.

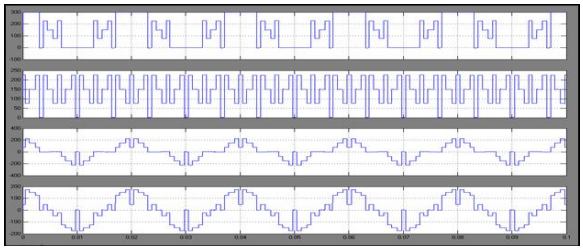


Fig. 6. Simulated waveforms of Vab at different modulation indices for the proposed inverter: (a)Ma =0.9, 1.05, and 1.15 and (b)Ma =0.8 and 1.3.]can be expressed as

$$M = 6(N-1) \quad (15)$$

2) The magnitude of dc voltage supply used in each and every cell in a particular inverter is obtained as follows:

$$V_{dc1} = V_{dc} \quad (16)$$
$$V_{dc2} = 2V_{dc} \quad (17)$$
$$V_{dcn} = nV_{dc} \quad (18)$$

3) By making a binary (power of 2) relationship between the dc supplies of the CHB structure as follows

$$V_{dc1} = 2^{(0)}(V_{dc}) \quad (19)$$
$$V_{dc2} = 2^{(1)}(V_{dc}) \quad (20)$$

TABLE I V
COMPARISON OF THE MAXIMUM NUMBER OF VOLTAGE LEVEL WITH THE REQUIRED VALUE OF DC VOLTAGE SUPPLIES AMONG THE PROPOSED METHODS

Number of cells	1st method			2nd method			3rd method		
n	*N*	*M*	*Vfix*	*N*	*M*	*Vfix*	*N*	*M*	*Vfix*
2	4	18	*3Vdc*	5	24	*4Vdc*	5	24	*4Vdc*
3	5	24	*4Vdc*	8	42	*7Vdc*	9	48	*8Vdc*
4	6	30	*5Vdc*	12	66	*11Vdc*	17	96	*16Vdc*
5	7	36	*6Vdc*	17	96	*16Vdc*	33	192	*32Vdc*
6	8	42	*7Vdc*	23	132	*22Vdc*	65	384	*64Vdc*

2) Since the second and third methods use the asymmetrical structure of CHB, the proposed inverter can reach the required output voltage and the maximum number of voltage levels such as 5, 8, 9, 12, 17,...with less number of dc voltage supplies and power electronic components.

Comparison study

In order to investigate the capability of the suggested configuration, the proposed inverter is compared with different types of multilevel inverters such as NPC, FC, and CHB. It is evident that the suggested three-phase N-level multilevel inverter can considerably minimize the required number of power components. For the same number of output voltage levels(N≥4),Table V explains the required number of dc voltage supplies ,switches, clamping diodes, control signals, and balancing capacitors of the proposed N-level inverter compared with three existing inverters NPC, FC, and CHB.

TABLE V
COMPARISON OF THE PROPOSED N-LEVEL INVERTER WITH THE EXISTING INVERTERS

Converter type	NPC	FC	CHB	Proposed		
				1st method	2nd method	3rd method
Switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Gate drivers	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$
Diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Clamping diodes	$6(N-2)$	0	0	0	0	0
DC supplies	$N-1$	$N-1$	$3(N-1)/2$	$N-1$	$1+[(\sqrt{8N-15}-1)/2]$	$1+Log_2(N-1)$
Clamping capacitors	0	$3(N-2)$	0	0	0	0
Control signals	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$

As shown in Fig. 8,it can be noticed that nearly more than two-thirds of number of switches can be counted out as N increases.

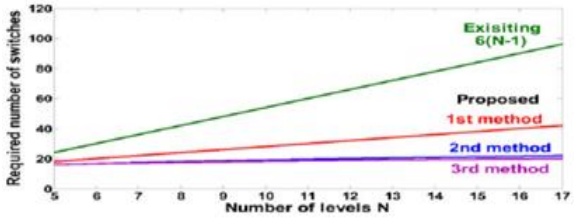


Fig. 8. Comparison of required number of switches among existing inverters and the proposed topology

For instance, at the same number of voltage levels N=17, and compared with the existing multilevel inverters which require 96 switches, the required number of switches for the proposed inverter is less since it requires 42 switches based on the first method, 22switches based on the second method, and 20 switches based on the third method.

It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are involved, the semiconductor devices expenses are considerably recovered.

Power conversion efficiency and total harmonic distortion (THD%):

In order to determine the efficiency of the proposed inverter, it is necessary to determine the value of conduction and switching power losses generated by the semiconductor components. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: conduction loss (Pcon) and switching loss (Psw)as follows:

$$P_{Sw\_IGBT} = \frac{1}{T}\int_0^T E_{on}(t)dt + \frac{1}{T}\int_0^T E_{off}(t)d(t) \quad (21)$$

$$P_{sw-diode} = \frac{1}{T}\int_0^T E_{rr}(t)dt(22)$$

Where Eon(t)is a turn-on loss and Eoff(t) is a turn-off loss. Switching losses Eon(t) and Eoff(t)are experienced during the ON and OFF states, respectively.

Conduction power losses of IGBT and diode are approximated based on their forward voltage drops Von IGBT, Von diode, and the instantaneous current i(t) flowing through IGBT or diode. The total losses P t are expressed as follows:

$$P_t = P_{con} + P_{sw}(23)$$

Once the total semiconductors losses Pt in the introduced inverter are defined, the relative inverter efficiency is determined based on the following expression:

$$\eta\% = \frac{P_{out}}{P_t + P_{out}} * 100 \quad (24)$$

Therefore, the conduction and switching power losses for the inverter switches and diodes can be estimated. The efficiency of the proposed inverter is estimated while the input voltage is raised in small steps. Fig. 9(a) depicts the estimated value of efficiency over a wide range of the output power. It is a result of more power being effectively transferred with respect to the power losses. Furthermore, the power losses distribution among the inverter's legs and the CHB cells are shown in Fig. 9(b). The estimated value of efficiency and power losses distribution of the NPC multilevel inverter are shown in ig. 9(c) and (d).

TABLE VI
Proposed and the existing topologies rating requirements per level n

Proposed inverter	Main bridge Q1 ~ Q6 D1a ~D2c	Bidirectional switches S1 to S6 D1 to D6	Cascaded half-bridge switches T1i to Tn2			Converter type	NPC	FC	CHB
			1st method	2nd method	3rd method	switches voltage rating	Vdc	Vdc	Vdc
Component voltage rating	(N-1)Vdc	(N-2) Vdc	Vdc	nVdc	$2^{(n-1)}$ Vdc	Clamping diode voltage rating	Vdc	0	0
						Clamping capacitor voltage rating	0	Vdc	0
Active Component current	IL	IL	IL	IL	IL	Active component current	IL	IL	IL

TABLE VI I
CONDUCTING DEVICES OF THE PROPOSED INVERTER PHASE A

Current	Conducting Devices Phase *a*. Fig. 1(a)	*Vag*	Conducting Devices Phase *a*. Fig. 1(b)	*Vag*
Ia > 0	Q1	+4*Vdc*	Q1	+4*Vdc*
	T1, T3, S2, Da2	+3*Vdc*	T1, T3, S2, Da2	+3*Vdc*
	Dz2, T3, S2, Da2	+2*Vdc*	Dz2, T3, S2, Da2	+2*Vdc*
	T1, Dz4, S2, Da2	+*Vdc*	T1, Dz4, S2, Da2	+*Vdc*
	D2, Da2	0	D2	0
Ia < 0	D1, Da1	+4*Vdc*	D1	+4*Vdc*
	Dz1, Dz3, S1, Da1	+3*Vdc*	Dz1, Dz3, S1, Da1	+3*Vdc*
	T2, Dz3, S1, Da1	+2*Vdc*	T2, Dz3, S1, Da1	+2*Vdc*
	Dz1, T4, S1, Da1	+*Vdc*	Dz1, T4, S1, Da1	+*Vdc*
	Q2	0	Q2	0

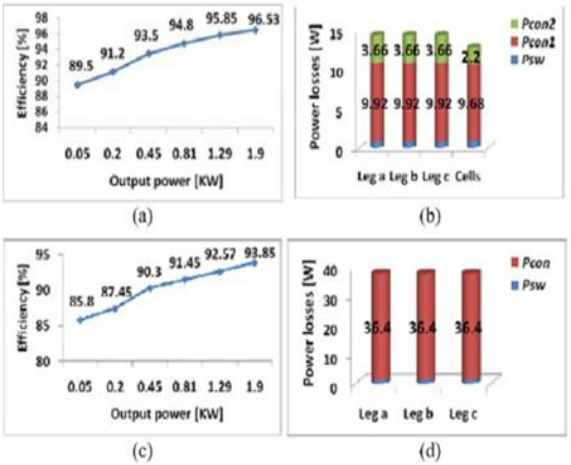


Fig. 9. Power loss and efficiency comparison. For the proposed inverter: (a) output power versus efficiency, (b) Pcon and Psw distribution among legs a, b, c, and CHB cells for Ma=1andPout=1.287 kW. For the NPC inverter: (c) output power versus efficiency and (d)Pcon and Psw distribution among leg sa, b, and c for Ma =1andPout=1.285 kW maximum estimated efficiency of the NPC multilevel inverter is 93.85%. At the same operating pointPout≈1.287 kW and compared with the estimated value of Pt proposed=3×14.4+12.78≈55.9 W generated by the proposed inverter, the estimated value of P generated by the NPC multilevel inverter is two times higher.

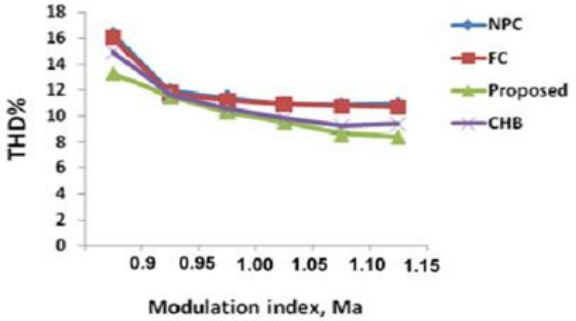


Fig. 10. NPC, FC, CHB, and proposed inverter: line-to-line voltage THD% versus Ma.

Moreover, the proposed inverter has been tested under different modulation indices (Ma =0.9, 1, and 1.15). THD% of the output voltage can be calculatedby

$$THD\% = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} * 100\% \quad (25)$$

Where V1 and Vk are the fundamental component and harmonic order, respectively. NPC, FC, and CHB multilevel inverters have been tested under the same operating conditions. The proposed inverter essentially adds the attractive aspects of the traditional two-level inverter such as less power components, simple working principle, and minimum conduction power loss to the main advantages of the multilevel inverter such as low THD% and high output voltage quality.

$$\eta\% = \frac{P_{out}}{P_{in}} * 100 \quad (26)$$

Where Pin and Pout are the inverter input and output power, respectively. The digital meter was utilized to measure Pin and Pout. The efficiency takes values around 88% under low power conditions. However, better efficiency is attained at higher power as 95.2% is the measured efficiency at 1.9 kW.

CONCLUSION

This paper presents an optimized configuration of a 3-ϕ MLI with minimum number of switches. The proposed system eliminates the CMV and high frequency voltage transition in between the load neutral and source terminal points. A new topology of the three-phase five-level multilevel inverter was introduced. The fundamental frequency staircase modulation technique was comfortably employed and showed high flexibility and simplicity in control. The proposed configuration was extended to N-level with different methods. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation technique can be also implemented. The proposed configuration was obtained from reduced number of power electronic components. Therefore, the proposed topology results in reduction of installation area and cost. By using the simulation results we can analyze the proposed method.

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