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DESIGN AND SIMULATION OF A FLOATING BRIDGE FOR OPEN-ENDED WINDING MOTOR DRIVE APPLICATIONS

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ABSTRACT- In this paper a dual two-level inverter is presented which reduces the size and weight of the system for an open end winding induction motor drive application. This paper presents a dual three phase open end winding induction motor drive. The drive consists of a three phase induction machine with open stator phase windings and dual bridge inverter supplied from a single DC voltage source. The aim of this topology is to eliminate the requirement for a bulky isolation transformer whilst achieving multi-level output voltage waveforms. To achieve multi-level output voltage waveforms a floating capacitor bank is used for the second of the dual bridges. The capacitor voltage is regulated using redundant switching states at half of the main dc link voltage. This particular voltage ratio (2:1) is used to create a multi-level output voltage waveform with three levels. The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. A modified modulation scheme is used to improve the waveform quality of this dual inverter. This paper also compares the losses in dual inverter system in contrast with single sided three-level NPC converter. By using the fuzzy controller for a nonlinear system allows for a reduction of uncertain effects in the system control and improve the efficiency. By using the simulation results we can analyze the proposed method.

Index Terms—Field-oriented control (FOC), floating bridge, open-end winding induction machine, fuzzy logic controller, space vector.

I. INTRODUCTION

Multilevel inverters can produce an output voltage waveform having a large number of steps with low harmonic distortion [1]. They can also reduce the stress on the switching devices as higher levels are synthesized from voltage sources with lower levels. Multi-level converters have lower dv/dt and reduced harmonic distortion along with lower semiconductor switching device blocking voltage requirements, thus multi-level converters are advantageous in medium voltage, high power or low voltage, high frequency applications [2]. Among the cascade converters, dual two-level inverter topology has received attention due to the simplicity of the power stage and the arrangement's fault tolerant capacity [3]. Traditional dual two-level inverter topologies use two standard three-phase inverters to achieve a multi-level voltage output. This topology does not have the neutral point fluctuations found in NPC converters, uses fewer capacitors than the flying capacitor topology and requires fewer isolated supplies than H-bridge converters. Dual inverters are more reliable, because in case of a failure in one converter the outputs of the converter can be short-circuited and the system can then operate as a standard single sided three phase inverter[14].

A Dual inverter scheme with asymmetrical DC link voltages for the open-end winding induction motor is capable of producing a 4-level PWM waveform with reduced switching ripple for the motor phase voltage. The traditional dual inverter topologies (using two isolated dc sources) has been analyzed [4], with different space vector modulation schemes used to generate the multi-level output voltage waveforms.

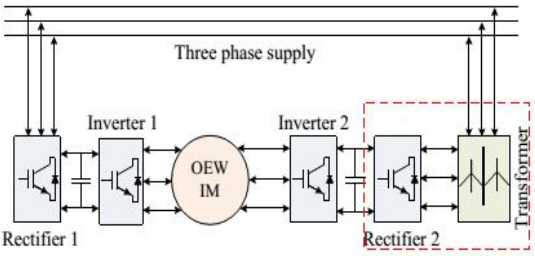


Fig. 1. Conventional open end winding IM drive topology.

A block diagram of a traditional open phase load and converters is shown in Fig. 1. It is possible to use a single supply for the dual inverters with a common mode elimination technique. These topologies use specific switching combinations that produce equal common mode voltages which cancel at load terminals. A reduction in the number of voltage levels and lower dc bus voltage utilization are the main disadvantages of this variation of the topology. A modulation technique to balance the power flow between the two inverters in a dual inverter system has also been proposed. The floating capacitor bridge topology along with a suitable

control scheme to allow the supply of reactive power was introduced.

The advantages of dual bridge inverter with respect to single ended inverters include:

• Improved availability because fault tolerance can be introduced.

• Reduced voltage blocking requirements for some of the power semiconductors

• Inverters can share switching events leading to lower individual device commutation frequencies.

• Reduced switching losses for a given output waveform quality

To compensate for supply voltage droop in order to keep the drive operational in constant power mode. This topology uses a floating capacitor bridge to offset the voltage droop in high speed machines. To remove the isolation transformer and achieve multilevel output voltage waveforms, a dual inverter with a floating capacitor bridge is considered [5]. A circuit topology is analyzed which is used as a three-level open end winding induction motor drive. This topology uses dual inverters with only one DC voltage source at the primary side of the converter. The voltage across the floating capacitor bank is controlled using the redundant switching vectors along with a modified SVM scheme which avoids unwanted voltage levels in the phase voltage waveforms during the dead-time intervals, thus improving the overall waveform quality.

II. PROPOSED SYSTEM

A. Floating capacitor bridge inverter

The floating bridge capacitor dual inverter based topology has been analyzed for different applications. The topology can be used to supply reactive power to a machine and to compensate for any supply voltage droop, but the possibility of multi-level output voltage waveforms were not considered. A control scheme to charge the floating capacitor bridge along with multi-level output voltage waveforms has been presented.

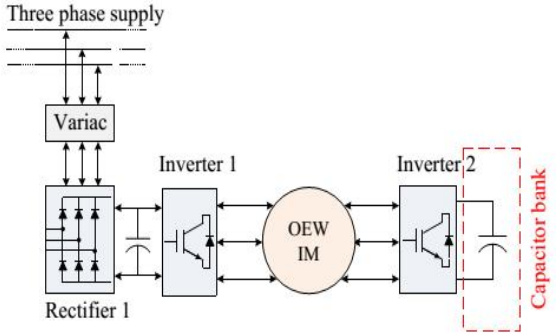


Fig. 2. Block diagram of proposed floating bridge topology.

Fig. 2 shows a block diagram of the dual inverter with a floating bridge and associated capacitor. In this method the main converter works in six step mode and the floating converter is called conditioning inverter as it is improving the waveform quality. The work described in this paper is to control the voltage across the floating inverter bridge capacitor using the redundant switching states, therefore removing the need for any isolation transformer and allowing the converter to achieve multi-level output voltage waveforms.

The use of a dc link voltage ratio of 2:1 allows the dual bridge inverter to produce up to a three levels in the output voltage waveform. The power stage of the proposed topology is shown in Fig.3.

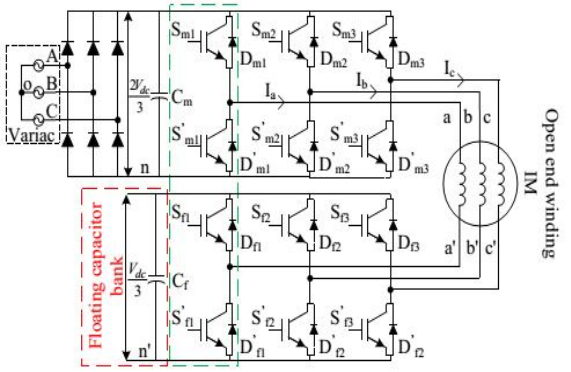


Fig. 3. Power stage of the floating bridge topology (the floating capacitor is charged to half of the main DC link voltage).

B. Principles of operation

In order to show how the floating capacitor can be charged and discharged the possible switching states are analyzed. The space vector diagram for the topology is shown in Fig.4, which is derived by assuming that both converters as being supplied from isolated DC sources with a voltage ratio of 2:1.

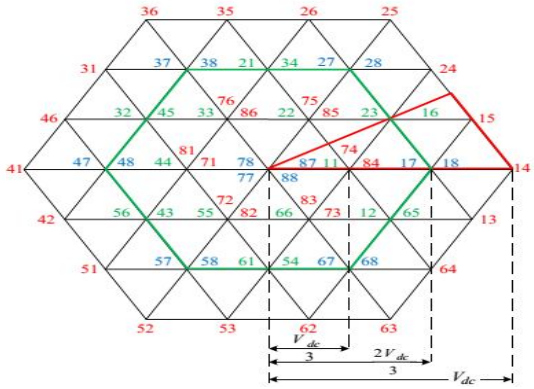


Fig. 4. Space vector of dual two-level inverter (source ratio 2:1).

In Fig.4 the red numbered switching combinations discharge the floating capacitor, while the green numbered switching combinations charge the floating capacitor. The blue numbered switching

combinations hold the last state of capacitor and are therefore neutral in terms of the state of charge of the floating capacitor. As an example state (74) shown in Fig.5 gives the switching sequences for both converter's top switches 7 (1 1 1) represents the top three switches for main inverter and 4 (0 1 1) represents the switching states for top three switches of the floating converter.

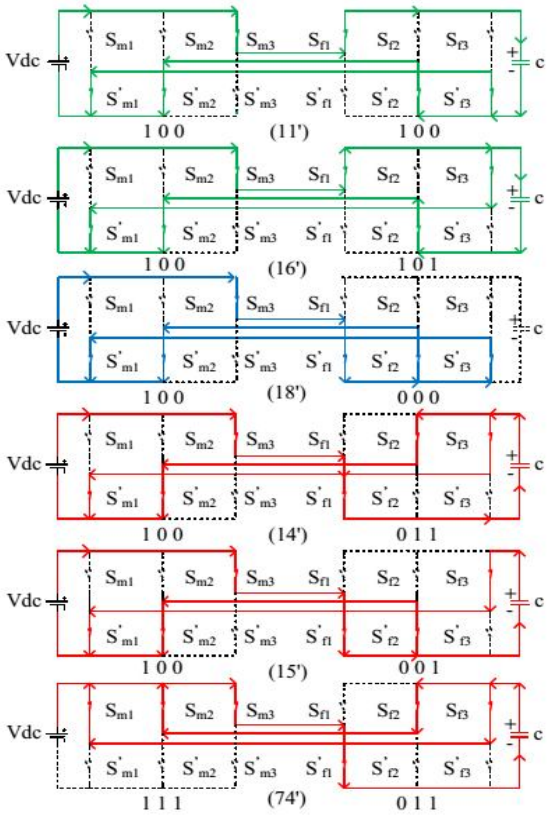


Fig. 5. Current flow for different switching state

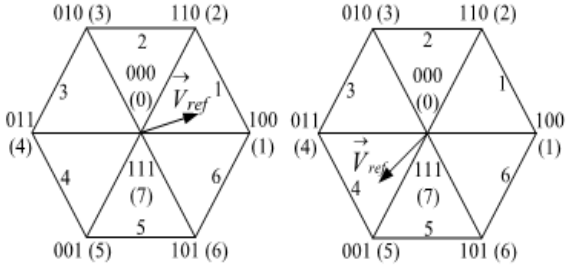
It can be seen from the Fig. 5 that combinations (11) and (16) will direct the current through the positive to negative terminal of the floating capacitor thus will act to charge the capacitor. It is evident from Fig. 4 that if the reference voltage is in outer hexagon then there are only two switching combinations in each sector to charge the floating capacitor. During inductive load operation capacitor discharge rate will be slower and will cause overcharging if the reference voltage lies in outer hexagon. Also, due to lack of charging states, the floating capacitor will discharge if the machine is drawing active power. To avoid these two phenomenon a restriction has to be imposed on modulation index. As a result the maximum useable number voltage levels across the load will be reduced to nine (thirteen for isolated sources) along with a slightly lower than ideal DC bus voltage utilization. Therefore the floating capacitor can charge to half of the main DC link capacitor voltage only if the modulation index (m) is limited as shown in equation

$$m = 0.66 \quad (1)$$

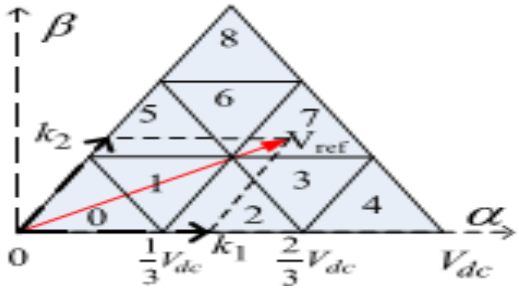
The dual inverter with a zero sequence elimination technique also uses single supply with 15% reduction in DC bus utilization and can achieve five-level voltage across the load

C. Modulation strategy

A decoupled space vector modulation strategy has been used for this dual inverter floating bridge topology. Switching combinations are selected in such a way that the average generated voltage for each of the converters is 180 degree phase shifted from the other [Fig.6 (a)]. These voltages will then add up at load terminal to match overall voltage reference [Fig.6 (b)]. The dual inverter with unequal voltage sources will show a different characteristic, instead of clamping the output voltage to one of the voltage levels before or after the dead-time interval voltage levels, it clamps the output voltage to some other voltage levels. This is true for simultaneous switching for each phase legs of the converters.



(a)



(b)

Fig. 6. (a) Space vector diagram of individual converter (not in scale). (b) Space vector diagram of the dual inverter system with sourece ratio of 2:1

For an example, consider phase legs inside green dotted line in Fig. 3 for positive load current (current flowing from main to floating converter). If the top switches of the legs (Sm1 & Sf1) are on then the load current will go through switch Sm1and diode D f1. Now, if both legs go to its dead time at the same time the load current will change direction and will go through diode D ' m1 and diode D f1 . Finally when both the converter legs bottom switches (S ' m1

& S ' f1) turned on current will go through diode D ' m1 and switch S ' f1 . It is clear that during dead-time interval, voltage level is different to the voltage levels before and after the dead-time interval. A generalized solution is shown in Fig. 7 for positive load current.

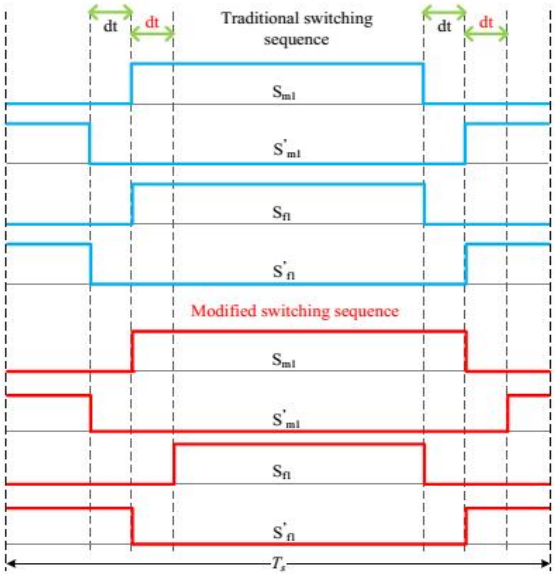


Fig. 7. Delayed dead-time intervals in both converters when current direction is positive.

It can be seen from the Fig. 7 that the pulses are delayed depending on the switching states transitions. Table I shows the generalized solution for positive and negative load currents to avoid the unwanted voltage levels.

TABLE I
DELAY TIME DEPENDING ON CURRENT DIRECTION

	Inv-1 Top	Inv-1 Bot	Inv-2 Top	Inv-2 Bot
I>0	Turn off	Turn on	Turn on	Turn off
I<0	Turn on	Turn off	Turn off	Turn on

Due to the modified switching sequences, the current direction does not change during the dead-time. The state of the floating capacitor will depend on the current just before the occurrence of dead-time interval. As an example, if the capacitor was charging then it will keep charging when the converter is in dead-time period. The value of dead-time is too small for the any overcharge or discharge to change the capacitor voltage drastically.

III. FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

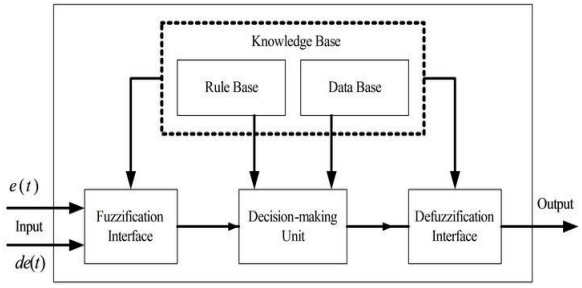


Fig.7.Fuzzy logic controller

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

TABLE I: Fuzzy Rules

Change in error	Error						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (2)$$

$$CE(k) = E(k) - E(k\text{-}1) \quad (3)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C] \quad (4)$$

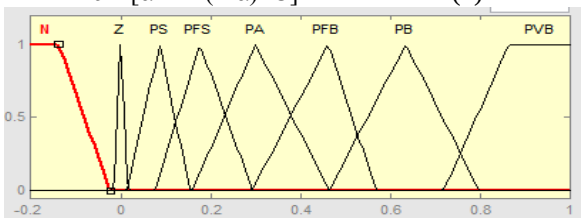


Fig 8 input error as membership functions

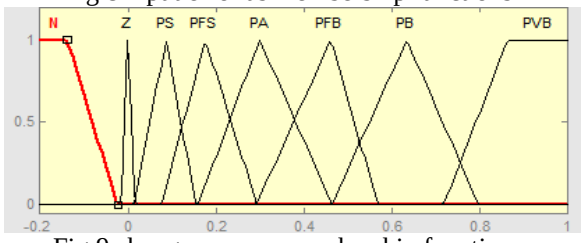


Fig 9 change as error membership functions

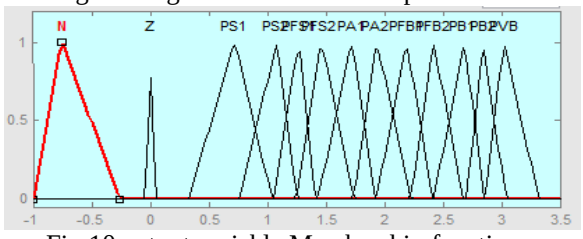


Fig.10.output variable Membership functions

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

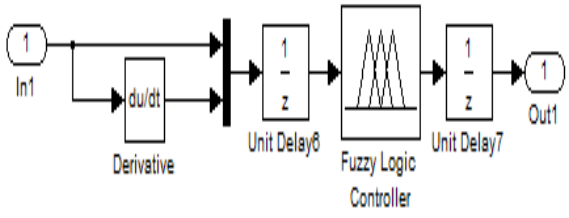


Fig 11.fuzzy logic controller in simulation

III. SIMULATION RESULTS

Results from the converter operating as an open loop v/f motor drive are presented to show the converter operation.

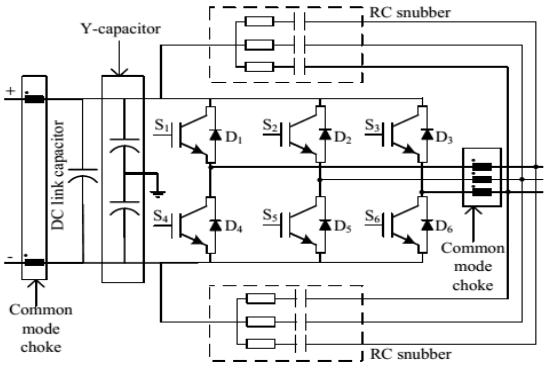


Fig.12. Power stage of the two-level converter.

A power stage diagram of the experimental two-level converter is shown in Fig.9. The parameters of the converter and machine are provided in Table III.

TABLE III
LOAD AND POWER CONVERTERS PARAMETERS

Induction motor		
Stator resistance	Rs	1.4 Ohm
Rotor resistance	Rr	1.02 Ohm
Stator leakage inductance	Lls	0.0115 H
Rotor leakage inductane	Llr	0.009258 H
Magnetizing inductance	Lm	0.2258 H
Power converter		
Main DC link	Vdc	500 V
Floating DC link	Vf	250 V
Main DC link capacitance	Cm	1250 µF
Floating DC link capacitance	Cf	3250 µF
Gating pulses propagation delay		0.1 – 0.2 µs
Onboard Deadtime	Dt	4 - 4.1 µs
Snubber capacitance	Cs	0.7 nf
Output common mode inductance	Lo	5 µH

A. Loss comparison

The losses of the proposed dual inverter system are compared in this section. Three converter types were selected, a single sided three-level NPC, a dual two-level inverter with equal DC link voltage ratio and the proposed dual inverter topology. The device losses were calculated using semiconductor device characteristics selected according to required blocking voltage and current requirements of the topology as presented in table II.

TABLE II
DEVICE VOLTAGE RATING COMPARISON

		Number of IGBT (voltage rating)	Number of diode (voltage rating)	Number of diodes in rectifier (voltage rating)	Capacitor Voltage
3-L NPC		12 (485 V)	18 (485 V)	6 (970 V)	485 V
Dual equal voltage		12 (485 V)	12 (485 V)	12 (485 V)	485 V
Dual Floating bridge	*Main*	6 (970 V)	6 (970 V)	6 (970 V)	970 V
	Float	6 (485 V)	6 (485 V)	n/a	485 V

The loss calculations were in terms of switching and conduction losses for the power converters and in this comparison all other circuit losses were ignored. Fig. 10 shows the efficiency at full load (12 KW) with varying switching frequency. It can be seen from the figure that, for this particular load, dual inverter with equal dc link voltage ratio has better efficiency than the other topologies. The three-level NPC has six extra clamping diodes, thus the losses are higher

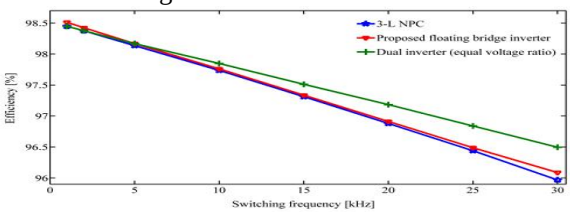


Fig. 13. Loss comparison in different power converter topologies.

The proposed floating bridge dual inverter has slightly better efficiency than three-level NPC but is less efficient than dual inverter with equal dc link voltage. The proposed floating bridge converter has two distinct switching patterns, one is for charging and the other is for discharging, thus it is difficult to maintain the minimum switch involvement for switching transitions.

B. Open loop v/f controlled IM drive

The results for open loop v/f controlled drive are presented from Fig. 11 to Fig. 12. Fig. 11 shows the no load voltage, current and floating DC link voltage, it can be seen that the drive charges the floating capacitor to required value and the converter achieves a multi-level output voltage waveform. To validate the open loop performance of an IM drive a step load was applied to the machine, shown in Fig. 12.

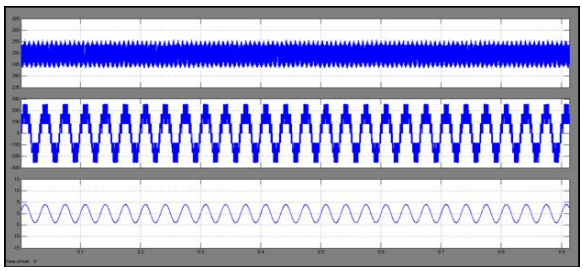


Fig. 14. Open loop v/f control IM drive Top to bottom : floating capacitor

The results presented in Fig. 15 were achieved using the modified switching pulses to avoid unwanted voltage level during the dead-time interval.

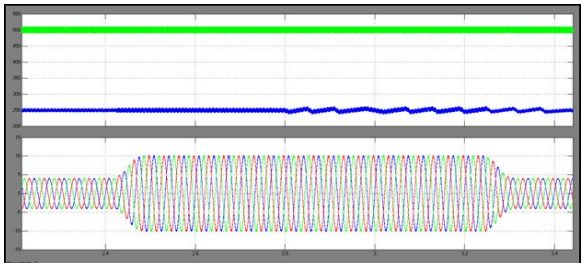


Fig. 15.Open loop v/f control IM drive Top to bottom : DC link voltages

A magnification of the leg voltages and the phase voltage of the converters are shown in Fig. 16 with no modification to the gating pulses. The leg voltages and phase voltage is plotted in Fig.17 after the introduction of the modified switching pulses, showing that the leg voltages are changing state at the same time and spike duration is shorter.

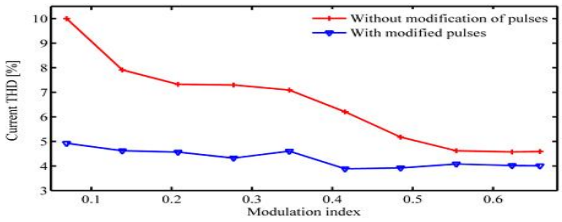


Fig. 16. Current harmonic distortion.

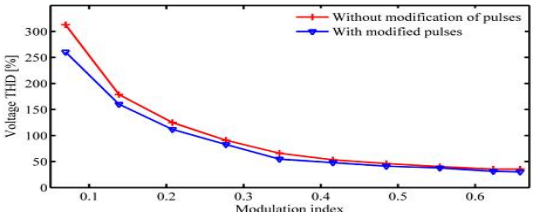


Fig. 17. Voltage harmonic distortion.

A simplified block diagram of the field oriented control system is presented in Fig. 18.

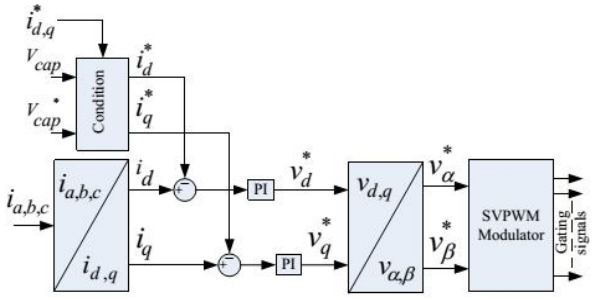


Fig. 18. Block diagram of vector control drive.

The algorithm also protects the system after the speed command is set. The controller will shut down the system if the capacitor voltage deviation is more than +- 15% of the demand value. A flow chart for this algorithm is shown in Fig. 19.

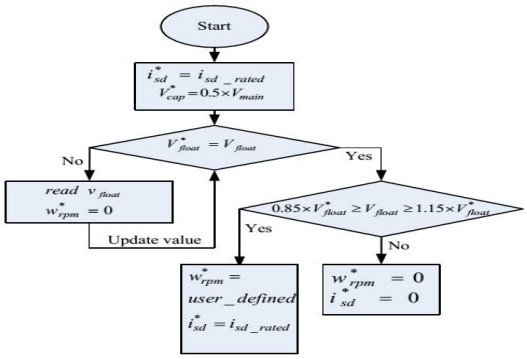


Fig. 19. Floating capacitor charging and protection algorithm

Initial charging of the capacitor is presented in Fig.20. The amplitude of the magnetizing current reference * d i may not be the rated value. After magnetization process was done, a step reference voltage was applied to show the charging dynamics of floating capacitor. It can be seen from Fig.20 that capacitor tracks the reference value and reaches steady state within 1.5 seconds.

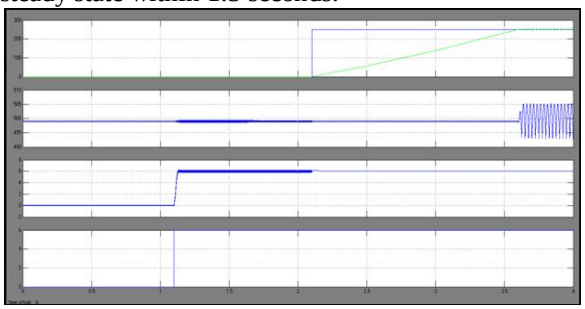


Fig.20. Initial charging of floating capacitor after machine is magnetized.

Top to bottom: floating capacitor voltage and reference, main dc link voltage, d-axis current and d-axis current reference. The capacitor voltage reaches steady state, a step demand speed reference of 700 RPM was applied. The response of the controller is shown in Fig. 21.

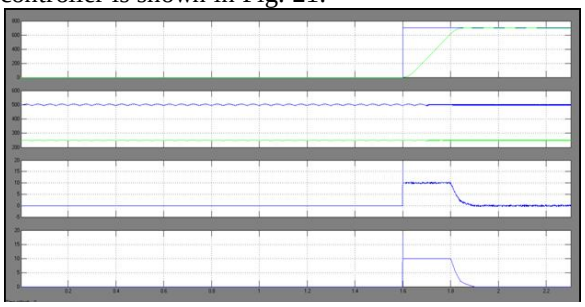


Fig. 21. FOC response of no load speed to a step reference speed command.

Top to bottom: rotor speed with reference, floating capacitor and main dc link capacitor voltage , q-axis current and referece q-axis current

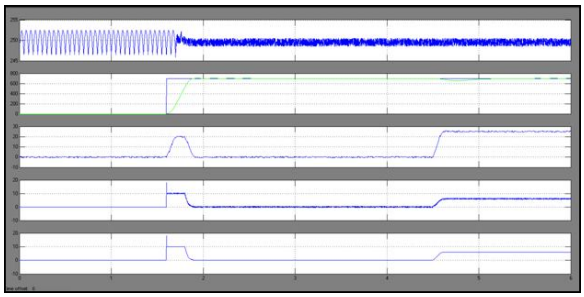


Fig. 22. FOC response to a step load applied after the speed reaches steady state.

Top to bottom: floating capacitor voltage, rotor speed, electromagnetic torque, q-axis current and reference q-axis current.

The reference torque current iq* is generated from the speed loop steps up immediately to counter the load torque, as shown in Fig. 23.

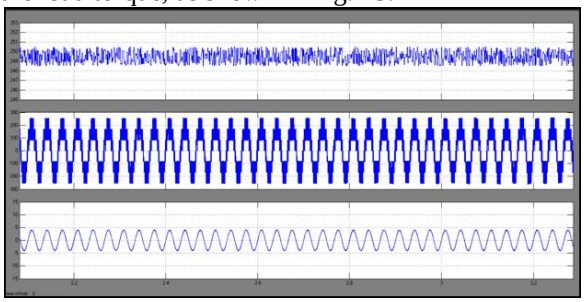


Fig. 23.Phase voltage and current under FOC when machine is loaded.

Top to bottom: floating dc link voltage, phase voltage Vaa', and phase current Ia.

IV. CONCLUSIONS

This paper presents a dual three phase open end winding induction motor drive. The drive consists of a three phase induction machine with open stator phase windings and dual bridge inverter supplied from a single DC voltage source. The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. The proposed system charges the floating bridge capacitor to a ratio of 2:1 with respect to main bridge DC link voltage amplitude. This particular DC link voltage ratio allows the converter to achieve multi-level output voltage waveform. The floating DC link voltage is kept at a constant voltage by the means of charging and discharging the floating bridge capacitor. This is achieved by selecting between the charging and discharging redundant states of the converter. An open loop v/f control drive was implemented to validate the performance of the capacitor control. The dynamic performance of the proposed system was evaluated using a close loop field oriented controlled motor drive, the results showed that the proposed topology achieves multi-level output voltage waveforms. The aim of this

topology is to eliminate the requirement for a bulky isolation transformer whilst achieving multi-level output voltage waveforms. By using the fuzzy controller for a nonlinear system allows for a reduction of uncertain effects in the system control and improve the efficiency. By using the simulation results we can demonstrate that this topology has potential for applications where size, weight, losses and redundancy are important, for example in aerospace, EV or HEV motor drives.

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