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Optimized Implementation of Mixing Drivers in Clock-Tree for Power Supply Noise Reduction

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ABSTRACT: In a synchronous clock distribution network with negligible skews, digital circuits switch simultaneously on the clock edge; therefore they generate a lot of substrate noise due to the resulting sharp peaks on the supply current. A solution is to split a large design in different clock regions and introduce intentional clock skews between them, while taking the timing constraints into account. In this paper we present a complete design flow to optimize the clock tree for less substrate noise generation in large digital systems. It proposes a technique to assign combinatorial cells and flip-flops to the clock regions. It also takes into account the impact of unintentional clock skew such as jitter on the computed skews inorder to assure a robust design. During the optimization, it uses compressed supply current profiles to improve the CPU time. Experimental results show more than a factor of two reduction insubstrate noise generation from large digital circuits of which the skews are optimized.

INDEX TERMS: deep submicron, power modeling and estimation, ground bounce, substrate noise, clock skew, low-noise digital design, mixed analog-digital ICs

I. INTRODUCTION

Substrate noise is a major obstacle for mixed-signal integration where it is mainly caused by switching-induced ground bounce in the digital domain [1]. In large digital circuits, high peaks on the supply current create power-supply noise (Ldi/dtnoise) in the supply network. The part of this noise on the VSSrail is the so-called ground bounce. Decreasing the peak and the slope of the supply current caused by the switchings of digital circuits will reduce the ground bounce generation and therefore the substrate noise. Such decrease can be obtained by introducing different skews to a clock network driving a synchronous digital system, creating different clock regions (Fig. 1). The use of intentional clock skew for noise reduction has been reported previouslyfor reducing the peak current [2]and the ground bounce [3][4]. In prior approaches, the skew of every individual flip-flop was optimized (fine-grained skewing) ith out considering the communication power

penalty between many clock regions due to increasing number of switchings and due to extra delay buffers when fixing the hold-time violations (Fig. 2). The number of switchings can be higher if the timing difference between clock regions is substantially large, i.e. large skew values are needed for reducing the ground bounce. In this case, multiple-timed cells toggle more than necessary, therefore cause an increase in power. Power penalty can also be severe in designs that require large skew values when we implement the skew of a particular flip-flop by means of delay units. Fine-grained skewing may also require many iterations during the skew optimization process since the fidelity of the results cannot be guaranteed if the switching behavior of the circuit changes as a result of the new skew values. Limiting the number of clock regions significantly reduces CPU and memory requirements during the skew optimization process, since for a large digital system the required number of clock regionsis substantially less than the total number of the flip-flops. For all these reasons, we need a clustering algorithm that groups the flip-flops into clock regions before the optimization. For each clock region, a small amount of skew spread can still be allowed in order to minimize the number of clock buffers driving the flip-flops [5]. This could be an extension of our approach. Up to now none of the previous skew optimization approaches [2][3]gives a minimum (required) value for the number of clock regions, which is set by the relation between the major resonance frequency of the circuit and the rise/fall timeof the supply current. In this paper we consider this effect to design the optimal clock network [6]. In fact, we will show that after a required number of clock regions no further reduction of the ground bounce is achieved. We also use representative supply current profiles to optimize the clock skews since the use of the total transient data is not feasible for the clock skew optimization [6][7].

The cost function used for the optimization of the clock skews also yields more accurate results as compared to previous work, which uses some mathematical functions based on a triangular approximation of the supply current [2][6]. For synchronous systems, the spectrum of the substrate noise has peaks at multiples of the digital clock frequency. These peaks are shown to be the dominant components of the total supply current [7][8]. As a result, the optimization should be performed at each clock harmonic on the constraint space formed by the skews. This gives more optimal results. Additional constraints such as performance/race reliabilities of the clock are also introduced in the optimization in order to have a clock tree tolerant to process variations, which have also been addressed [9].

Two techniques to reduce digital substrate noise generation have been demonstrated in [7]: clock frequency modulation and intentional clock skews. The experimental

validation of the use of intentional clock skews in order to compare its effectiveness with the use of other low-noise digital design techniques such as decoupling has been presented in [8]. With respect to frequency modulation, in [7] we focus on the frequency spectrum analysis of the supply current in an effort to find the optimum settings for the modulating waveform. In this paper we particularly describe the clock skew optimization methodology where we highlight the following of our contributions: folding the supply current, determining the required number of clock regions, clustering the clock regions, and optimizing the clock skews.

II. Clock Skew Optimization for Reduction Of Substrate Noise

The clock skew optimization methodology consists of four major steps: (1) supply current folding (II.A) (2) finding a minimum (required) number of clock regions (II.B), (3) assignment of the digital cells to the clock regions (II.C), and (4) clock skew optimization (II.D). The methodology flow is given in Fig. 3with an indication of the main steps listed above. The different steps are now described in detail.

A. Supply current folding

For run-time efficiency of the clock skew optimization methodology, it is not possible to use the complete transient data of the supply current over a long time period. In this section we present an algorithm to generate the representative supply current profile(s) for each of the Mcurrent waveforms, where Mis the number of clock regions. Each clock cycle is discretized into Ntime intervals. For synchronous CMOS circuits, each cycle of the supply current in the time domain can be approximated by a triangular waveform (Fig. 4) where Ip, tr , and tf are the peak value, the rise time, and the fall time, respectively. The presented algorithm assures a certain maximum error bound on the parameters Ip, tr , and tf of the system supply current constructed by using the supply current profile(s) with respect to each cycle of the total supply current of each clock region. These representative supply current profiles will then be used to optimize the clock skews of the M clock regions.

B. Finding a minimum number of clock regions

Below a certain number of clock regions the substrate noise reduction by means of intentional clock skews may not be significant. In this section, we will find the required (minimum) number of clock regions in order to have a significant reduction in the substrate noise generation. Fig. 6illustrates the influence of tr and tfon the RMS value of the substrate noise voltage ([vSUB(t)] B RMS) due to a triangular-shaped supply current simulated in SPICE for a 25K-gates circuit in a 0.35 μm 3.3 V CMOS process. For each of the power/ground rails the circuit has a supply line inductance (Lp(g)) of 0.1 nH and a supply line resistance (Rp(g)) of 10 mΩ. The circuit has an extracted resonance frequency (fo) of 530 MHz and a damping factor of 0.19. The substrate noise voltage has been normalized to its maximum value that occurs at tr=tf =0 (where the supply current is a dirac impulse). We define the corner frequency (fc) of the supply current as the bandwidth of the supply current spectrum (see). Three regions are recognized ( ). (1) In the case when t Fig. 4 Fig. 6 r and tf are small, fc is much larger than fo. In this region, the power spectral density (PSD) of the supply current in the vicinity of fo does not change significantly by modifying tr and/or tf . (2) By increasing tr(tf), fc approaches fo and the iso-reduction lines become closely spaced. The

rate of reduction increases significantly because the main lobe of the supply current is shifting well below fo. (3) Decreasing fc even more makes the current waveform a band-limited signal. In the limit, the main lobe becomes infinitely small, i.e. only DC level remains. Lowering fc below fo will therefore bring a significant reduction in the substrate noise generation. This can be done by increasing the number of clock regions with skewed clocks. Without looking at the timing implications, the required minimum number of clock regions, M, is found by the ratio fc/fo. Choosing Mor more clock regions spreads the supply current uniformly over a time period of max(tr,t f)+tr+tf . This then sets the new corner frequency of the supply current at a frequency lower than the resonance frequency.

III. Proposed System

Clock-Tree and Power Supply Noise

The construction of clock networks as a part of a SoC design offers various topologies, such as spine, mesh, grid, and trees [9]. No matter what network topology is used at the system-level, the far-end local networks are implemented as trees. Shown in Fig. 4, an H-tree topology is very popular due to its symmetry and layout efficiency. It has been used by the

PowerPC processors family [23], [24], and it is supported by most clock-tree synthesis EDA tools. The elegancy of H-tree is also a source of considerable power-noise. Due to its symmetry, all the drivers at a given level of the tree will switch simultaneously [see Figs. 1(a) and 3(a)]. This results in a progressive sequence of coherent current peaks, cumulating to a large pulse as shown by the red waveform in Fig. 5. Flattening it will reduce both IR and voltage drops. The green waveform in Fig. 5 is resulted by the clock-tree proposed in our work, showing 40% peak reduction and smaller .

To ensure a robust signal, clock-trees usually employ LVT drivers, though those consume high leakage current. The coherence of the clock signal at tree's internal nodes ensures small skew at the sinks. An important question is whether the driver uniformity and symmetry of the clock-tree is necessary for small skew, or maybe it can be differently achieved. Our proposal breaks the clock-tree symmetry and uniformity paradigm as follows.

1) It replaces half of the LVT drivers by HVT ones.

2) It “disorders” the local peaks by locally mixing HVT and LVT drivers, thus spreading and smoothing the local current waveform.

3) It maintains acceptable clock signal slope and small skew at the sinks.

CHARACTERIZATION OFCLOCK-DRIVERS

The terms nodes and drivers are used interchangeably. The clock-tree construction algorithm employs a top-down and bottom-up traversals. The visit at a node requires iterative equation solution, which involves extensive delay and slope calculations. Using in-traversal SPICE simulations is unacceptably time consuming. We rather characterize each clock-driver beforehand

and then use characteristics data instead of simulations. This is far computationally efficient, whereas accuracy is hardly hurt. Our work used 40 nanometers TSMC process technology. The characterization takes place at PVT=TTT corner, where , and . The characterization runs extensive SPICE transient simulations, using a set of input slopes, ranging from 10 ps to 200 ps in steps of 8 ps, and a set of capacitive loads, ranging from 5 fF to 250 fF in steps of 50 fF. Each slope-load pair is simulated to obtain the following characteristics, shown in Fig. 5.

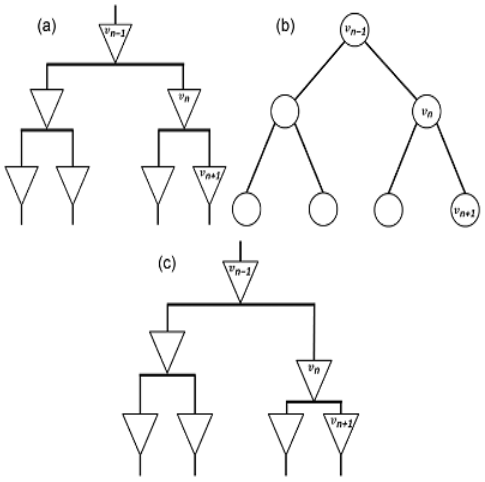

Fig 1 Clock-tree topology and modifications

Clock network comprises not only drivers, but also interconnects, strongly affecting the current waveform and the clock skew. The interconnect setting includes their sizing and where the drivers are located along those. The impact of interconnect is modeled in a closed-form expression shown subsequently. Consider three successive tree levels illustrated in Fig. 7(a) and the corresponding graph representation in Fig. 7(b). A driver at level of the tree is denoted by . Fig. 7(c) shows a modification of the physical location of within the tree. While some wires are shortened, others are lengthened. Fig. 8 models the delay changes incurring by drivers displacement. Considering three successive drivers, and, let the location of and be fixed, while is allowed to be displaced in between.

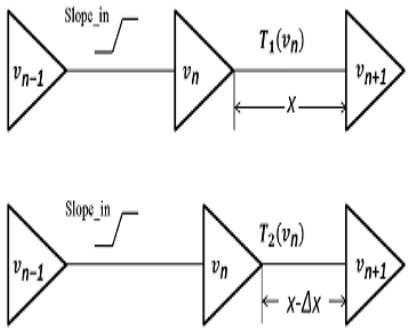

Fig 2. Delay modeling of driver isplacement.

Fig. 9 shows the SPICE delays in red, and their linear approximation in green for various drivers. The delay changes for HVT and half-size LVT clock-drivers are shown to linearly depend on their position across a wide range of wire lengths, as follows

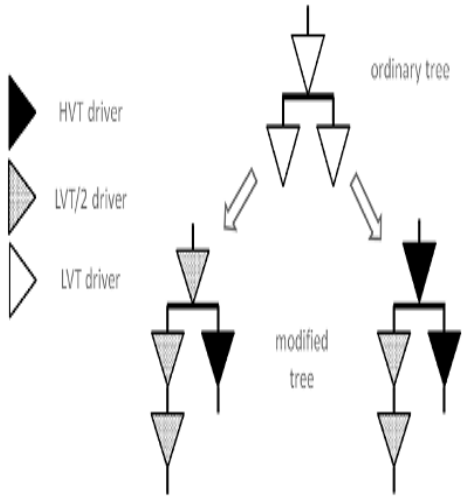

Fig. 3. Mixing LVT and HVT clock-drivers in a clock-tree

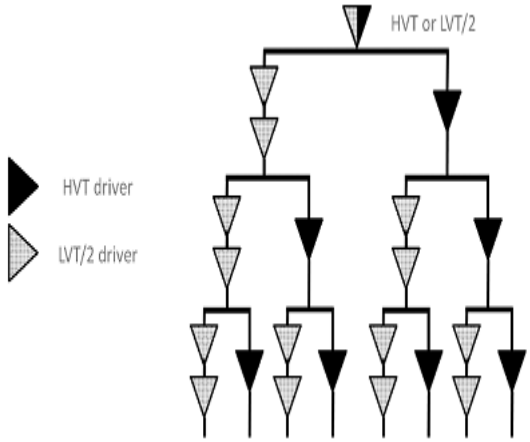

Fig 4.3-level clock-tree mixing HVT and LVT/2 drivers

Peak Current Reduction by Clock-Driver Mixing

` The peak current is reduced by misaligning the drivers' switching time, obtained by systematically mixing HVT and weak LVT drivers. The notation LVT/2 denotes a weak (half size) LVT driver. A fork of an ordinary clock-tree comprises only LVT drivers is illustrated in Fig. 11. We use instead the Fig. 11. Mixing LVT and HVT clock-drivers in a clock-tree. Fig. 12. 3-level clock-tree mixing HVT and LVT/2 drivers. two shown configurations, advised by experiments of various configurations. The replacement of an LVT driver by two LVT/2 ones has been shown to nicely spread the current pulse over time, while yielding sufficient dynamic range to tune-up the delays for achieving nearly zero skew. This is further shown in Figs. 13 and 14. For an -level tree with sinks, the structure proposed in Fig. 11 results in distinct root-to-sink paths, comprising a mix of HVT and LVT/2 drives. The leftmost path is purely LVT/2, whereas the rightmost is purely HVT. An example of 3-level tree is shown in Fig. 12. The clock-tree is assumed to be binary and balanced (the H-tree in Fig. 4 is such). This is a common assumption in the analysis of algorithms, which does not restrict the generality of the approach. A node of the tree is associated with the following parameters, derived along the tree traversal with the aid of the characteristic data of drivers.

1) : capacitive load driven by .

2) : propagation delay from the output of the parent to the output of its son .

3) : propagation delay from the tree's root to the output of .

4) : voltage slope at 's output.

While the peak current is reduced, the clock skew at the sinks, defined by the difference between the maximum and minimum root-to-sink latencies, should be maintained nearly zero to enable time-borrowing in the logic design. This could be obtained if the propagation delays from the parent in Fig. 11 to the far ends of its sons will stay equal, thus avoiding skew accumulation. Fig. 13 shows the response of the two branches, obtained by SPICE simulation. The magnified crossing point shows that their 50% to 50% delay difference is 3.6 ps, which is less than 0.5% of 1 GHz clock frequency. Similar behavior was observed for all the clock-drivers we used. Another important advantage is the smaller leakage current of the HVT, compared to LVT ones. The simulation inFig.13 use d equall ad sat the far ends of the two branches. This alone is not sufficient to ensure the equality of root-to-leaf delays, since the algorithm will later displace the location of the load drivers. This in turn changes the loads seen by the branches, breaking the delays equality. Such top-down blindness is being fixed by the second, fine-tuning bottom-up phase. Fig. 14 shows how the local peak current is reduced by the HVT and LVT/2 mix. The waveform in (a) is of a nominally sized LVT driver. The waveform in (b) is of two cascaded LVT/2 drivers and an HVT driver. The waveform in (c) shows the total current pulse drawn from the supply by the mix, presenting 43% reduction of the peak

IV. CONCLUSIONS

In this paper we have introduced an efficient clock skew optimization methodology for reducing the ground bounce (therefore substrate noise) in large digital circuits. The methodology splits the digital system in different clock regions and optimizes the clock skews between them to reduce the substrate noise generation. The required number of clock regions is computed based on the elimination of the major resonance frequency determined by the on-chip circuit capacitance and the supply line parasitics. The run-time of the optimization is improved by using supply current profiles, which can be used as periodic pulses for the epresentation of the total supply current. Additional constraints such as performance and race reliabilities have been introduced into the optimization in order to have a resulting clock tree tolerant to process variations.

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BIOGRAPHIES

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