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An Optimized Implementation of Booth-Encoded Wallace Tree Multiplier for FFT Computation in DSP Applications

Sankati Swathi[1] **A.Akhila**[2] **B. Nihar**[3]

swathiswa193@gmail.com[1] nihargopal2010@gmail.com[3]

[1]PG Scholar,Dept of ECE, Prasad Engineering College, Jangoan, Warangal, Telangana.

[2]Assistant professor, Dept of ECE, Prasad Engineering College, Jangoan, Warangal, Telangana.

[3]Assistant professor, Dept of ECE, Prasad Engineering College, Jangoan, Warangal, Telangana

Abstract - The squaring unit is an important one for different engineering branches like Digital Signal processing, Image processing and as well as the in the communication also. The low complexity and high speed hardware solution is essential one for now a day's communication system. The literature survey reports the either any one of the thing is taken into consideration for hardware solution like either low complexity or the high speed only. The proposed one aim is both factors are implemented simultationly using Vedic Mathematics. Direct computation of square of a given binary number consumes same amount of recourses of multiplication. Mathematical multiplication is an essential operation in any DSP calculation. In this paper, we propose an hardware architecture solution for the low complexity and high speed square unit using the Vedic mathematics principles. Electroencephalographic (EEG) signals are invariably used for clinical diagnosis and conventional cognitive neuroscience. This work intends to contribute to a faster method of computation of FFT for analysis of EEG signals to classify Autistic data.

Keywords—FFT, Multiplier, EEG

I. Introduction

Fourier transformation is the basis for the majority of the digital signal processing applications. The Fourier transform is a principle analytical tool that has its roots in such diverse fields as linear systems, optics, probability theory quantum physics, antennas, and signal analysis. Even with the tremendous computing speeds available with modern computers, the slow computation of DFT found relatively few applications because of the exorbitant amount of computation time. However, with the development of the Fast Fourier Transform (FFT), many facts of scientific analysis have been completely revolutionized. FFT finds applications in biomedical engineering, mechanical analysis, analysis of stock market data, geophysical analysis, and the conventional radar communication field. The development of fast algorithms usually consisting of special properties of the interest to remove redundant or unnecessary operation of a direct implementation. The Discrete Fourier Transform) (k X of a complex sequence) (n x where□ □ 1 ,.... 2 , 1 , 0 , N k n can be defined as

$$X(k)=\sum_{n=0}^{N-1}x[n]\ W_N^{kn} \quad (1)$$

$$x[n]=\frac{1}{N}\sum_{k=0}^{N-1}X(k)\ W_N^{-kn} \quad (2)$$

where,

$$W_N=e^{-j\frac{2\pi}{N}} \quad (3)$$

II. FFT USING FPGA

Vedic mathematics is mainly based on 16 sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. Digital signal

processing is one of the core technologies, in rapidly growing application areas, such as wireless communications, audio and video processing and industrial control. The number and variety of products that include some form of digital signal processing has grown dramatically over the last few years.

DSP has become a key component, in many of the consumer, communications, medical and industrial products which implement the signal processing using microprocessors, Field Programmable Gate Arrays (FPGAs), Custom ICs etc. DSP techniques have been very successful because of the development of low-cost software and hardware support. For example, modems and speech recognition can be less Expensive using DSP techniques. DSP processors are concerned primarily with real-time signal processing. Real-time processing requires the processing to keep pace with some external event, whereas non-real-time processing has no such timing constrain Fast Fourier transform (FFT) has an important role in many digital signal processing (DSP) systems. E.g., in orthogonal frequency division multiplexing (OFMD) communication systems, FFT and inverse FFT are needed.

The OFMD technique has become a widely adopted in several wireless communication standards. Today, various FFT processors, such as pipelined or memory-based architectures, have been proposed for different applications. However, for long-size FFT processors, such as the 2048-point FFT, the pipelined architecture would cost more area and power than the memory-based design. Hence, memory based approach as gained more and more attention recently in FFT processor designs for long-size DFT applications.

For the memory-based processor design, minimizing the necessary memory size is effective for area reduction since the memory costs a significant part of the processor. On the other hand, the FFT processor usually adopts on-chip static random access memory (SRAM) instead of external memory. The reason is the high-voltage I/O and the large capacitance in the printer-circuit-board (PCB) trace would increase power consumption for external memory.

III. Literature Survey

FAST Fourier transform (FFT) is the major block in orthogonal frequency division multiplexing systems. Ofdm has allocated in a large range of applications from wired-communication modems, such as digital subscriber lines (xDSL) [1], [2], to wireless-communication modems, like IEEE802.11 [3] WiFi, IEEE802.16 [4], [5] WiMAX or 3GPP long term evolution (LTE), to process baseband data. Inverse fast Fourier transform (IFFT) converts the modulated information from frequency domain to time domain for transmission of radio signals, while FFT gathers samples from the time domain, again converting them to the frequency domain.

Y.G.Li, J.H. Winters and N.R.Sollenberger[6] proposed multiple input multiple output (MIMO) devices, data throughput can be increased drastically. Hence MIMO-OFDM systems provide data rate and reliability in wireless communications. To handle “multiple” data streams, firstly the functional are to be duplicated for processing the giveninputs. Without a proper design, the complexity of FFT/IFFT processors in MIMO systems increases linearly with the number of data streams.

B. G. Jo and M. H. Sunwoo [8] proposed pipelines schemes, are the architectures most widely adopted for the

implementation of FFT/IFFT. From the memory access perspective, in-place memory updating schemes performs the computation in three phases: writing in the inputs, updating intermediate values, and reading out the results. In updating phase, the processor reuses the radix-r processor, such that a single radix-r butterfly is sufficient to complete N-point FFT/IFFT computation. Since each phase is non-overlapped, the outputs can be sequential or as requested. However, it is the non-overlapping characteristic that makes the butterfly idle in memory write and read phases, and the overall process is lengthy. Continuous-flow mixed radix (CFMR) FFT.

P. Y. Tsai and C. Y. Lin [9] utilizes two N-sample memories to generate a continuous output stream. One of the memories is used to calculate current FFT/IFFT symbols, while the other stores the previously computed results and controls the output sequence. Thus, when CFMR is used in MIMO systems, the required memory is increased in a trend proportional to 2×Ns, where Ns is the number of data streams. Such memory requirement may be forbidden if Ns is large, because the area of memory does not shrink as much as that of logic gates when fabrication technology advances, due to the use of sense amplify circuitry.

IV. Fast Fourier Transform Algorithm

Fast Fourier Transform is an algorithm to compute Discrete Fourier Transform which diminishes the number of computations for n-point radix from N 2 to N logN arithmetic operations. There are two methods to compute DFT through FFT algorithm, namely, Decimation-in-time (DIT) and Decimation-in-frequency (DIF) FFT algorithms. In Radix-2 DIT-FFT, input signal is decimated into even-indexed and odd-indexed values such that the series x(n) where, n=0, 1,2,…N changes to x(2r) and x(2r+1) where r=0,1,2,….N/2-1. In Radix-2 DIF-FFT, the x(n) series is broken into x(n) for n=0,1,2….N/2 -1 and x(n) for n=N/2, N/2+1,….N-1.

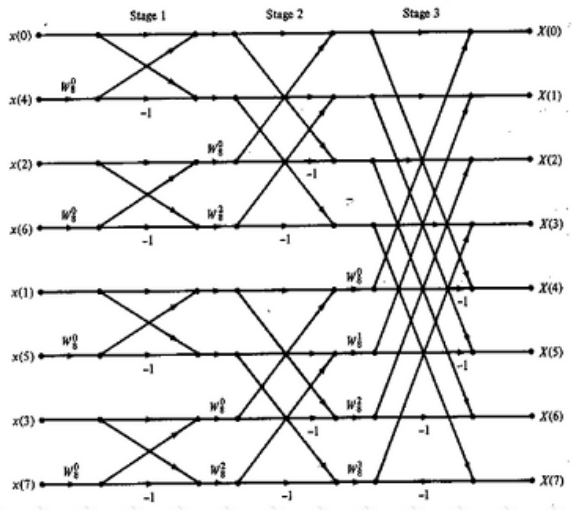

Fig. 1. Radix-2 8-point DIT-FFT algorithm

V. MULTIPLIERS

Multipliers have large area, long propagation delays and consume power. Therefore, low-power multiplier design has an important role in design of low-power VLSI systems. Power refers to number of Joules dissipated over a certain amount of time whereas energy is the measure of the total number of Joules dissipated by a circuit [9]. In digital CMOS design, the well-known power-area/power-delay product is commonly used to assess the merits of designs [9]. Any multiplier design involves 3 steps. They are i) partial product generation ii) partial product reduction and addition iii) final addition. The partial products are formed first either by using an algorithm or using AND gate for each bit of the multiplier with each bit of the multiplicand. The next step is reduction of these partial products. The third step is addition of the remaining partial products to yield the final product [9]. Hardware multipliers widely used are Booth Multipliers and Wallace Tree Multiplier. Area and Power parameters of Booth Multiplier

and Wallace Tree Multiplier are studied and their advantages have been incorporated to develop the concept of Booth-encoded Wallace Tree Multiplication.

A. Booth Multiplier

Booth Multiplier implements Booth Algorithm, named after its originator, A. D. Booth. This algorithm is implemented for signed multiplication of integers and can be extended to real numbers. Algorithm is based on recording the multiplier to a recorded value leaving the multiplicand unchanged [6] i.e. • Each '0' digit is retained in the recorded number until 1 is encountered on evaluating from LSB to MSB.

• Complement of 1 is inserted at every '1' digit in recorded number and all other succeeding 1's are complemented until a '0' is encountered.

• Then, replace the '0' with '1' and continue the process.

Two main drawbacks of Booth Algorithm are the inefficiency of the circuit when isolated 1's are encountered and difficulty in designing parallel multipliers as number of shift-and-add operations may vary. Hence Modified Booth Algorithm was developed by O. L. Macsorley. Modified Booth Algorithm is twice as fast as normal Booth Algorithm [4]. This modified Booth Encoding algorithm reduces the number of partial product rows to (N +2)/2 where N is the number of bits of Multiplier or Multiplicand.

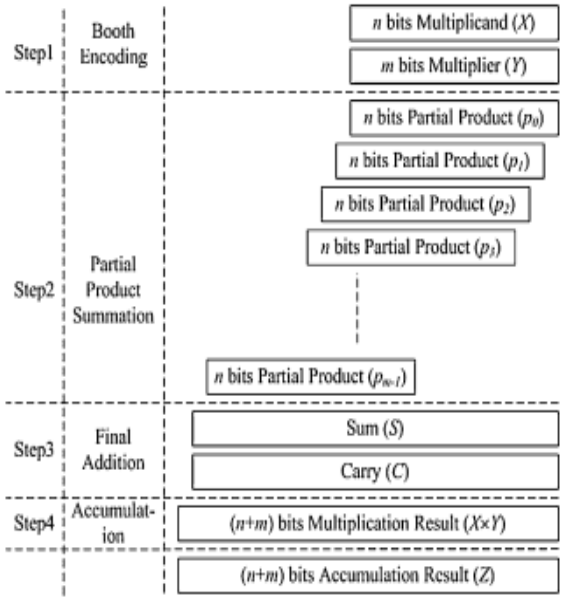

Fig. 2. Basic arithmetic steps of multiplication and accumulation.

B. Wallace Tree Multiplier

Wallace Tree Multiplier is one of the hardware multipliers used to accomplish high speed and low power multiplication to condense the number of partial products generated. There are two main techniques followed in designing Wallace Tree Multiplier. First technique is to consider all bits in each column at a time and compress them into two bits, namely, Sum and Carry. Second technique is to consider all bits in four rows at a time and compress them. Wallace Tree Multipliers use half adders, full adders, 4:2 and 3:2 compressors and a high speed adder [10]. Partial product generation, partial product addition and final addition are the three stages in a multiplier.

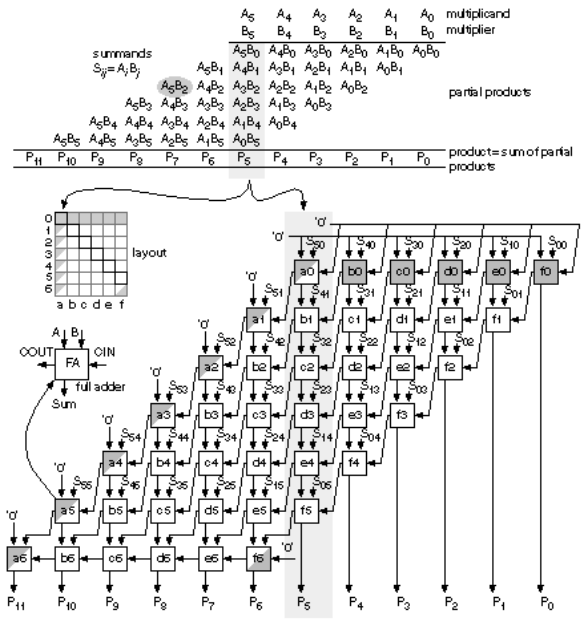

Fig 3: Wallace Multiplier

In Wallace Tree Multiplier, the multiplicand is multiplied by the multiplier, bitby-bit, to generate partial products. They are, then, added based on Wallace Tree structure to produce two rows of partial products which are finally added using any high speed adder. The critical path delay of Wallace Tree multiplier is proportional to the logarithm of the number of bits in the multiplier. Algorithm for Multiplication of two signed integers is as follows:

• Multiply (AND) each bit of one of the arguments,

• Reduce the number of partial products to two by layers of full adders and half adders (Compressors).

• Group the wires in two numbers, and add them with a conventional adder [9].

Wallace tree multiplication can be implemented only for signed integers and are avoided for low power applications as excess wiring consumes more power.

C. Booth-Encoded Wallace Tree Multiplier

Based on the comparative study of Area and Power parameters of Booth Multiplier and Wallace Tree Multiplier, Booth-encoded Wallace Tree Multiplier is chosen as an efficient multiplier for FFT computation. Table I. shows Area and Power performance parameters of the two multipliers which are coded in Verilog HDL and performance parameters are evaluated using IC Compiler tool from Synopsys Inc. Though Wallace Tree multiplier shows better performance in terms of Area and Power than Booth multiplier, its operation is limited to signed integers alone. As FFT computation in biomedical applications involves signed real numbers, Booth Algorithm is to be implemented for the multiplier.

TABLE I. PERFORMANCE PARAMETERS OF 4X4 BOOTH MULTIPLIER AND WALLACE TREE MULTIPLIER

Multiplier	Area(nm^2)	Power(μW)
Booth Multiplier	974.872	235.184
Wallace Tree Multiplier	600.868	180.504

Multiplication of the two operands, Multiplicand (MD) and Multiplier (MR) results in 2N bits for conventional multiplication. However, Booth encoded multiplier reduces number of partial products to (MD/2 -1) partial products [5]. Booth Algorithm is based on recording the multiplier to a recorded value leaving the multiplicand unchanged. It scans the multiplier operand and skips chains. It reduces the number of additions required to produce the result [4]. Booth-encoded Wallace Tree Multiplier has advantages of both Booth Multiplier and Wallace Tree Multiplier. This paper implements Booth encoding to increase speed of algebra by reducing number of partial products and Wallace Tree module for decreasing number of levels of addition.

1) Architecture of the Multiplier

In Booth encoded multiplier, number of partial products are reduced by grouping multiplier bits into pairs and selecting partial products from the set {0, M, 2M, 3M} where M

is the multiplicand. Modified Booth encoded multiplier, avoids the use of Carry Propagate Adder to calculate 3M, rather it utilizes Carry-Save-Adder. Thus, in Modified Booth Algorithm, number of partial products is reduced by a factor of two without a pre-adder to produce partial products [6]. Multiplier decoding is done such that multiples needed are in {0, M, 2M, 4M + -M} data set. These multiples can be generated using shift-and-complement methods. Fig.4 shows the architecture of Booth-encoded Wallace Tree Multiplier which consists of five blocks, namely, 2's Complement Generator, Booth Encoder, Partial Product Generator, Wallace Tree module and Carry Look-ahead Adder [7]. Booth encoder inspects each bit of the multiplicand and records the multiplier in terms of 0, 1 and complement of 1. As complement of 1 cannot be represented on hardware, operational equivalent of recorded multiplier is implemented based on Table II. Here, outputs of the encoder. x and z are defined as:

$$x = MR[i] \bullet MR[i-1] \quad (2)$$

$$z = MR[i] \oplus MR[i-1] \quad (3)$$

Where MR[i] and MR [i-1] corresponds to ith and i-1th bit of Multiplier, respectively. 2's complement generator takes the multiplicand MD as input and produces –MD as output .i.e. inverts all bits of multiplicand and uses a Ripple Carry Adder to generate 2's complement. Partial product generator generates appropriate partial products to be added in Wallace tree structure. Wallace Tree module adds all partial products. Addition is implemented using Carry Look Ahead Adder.

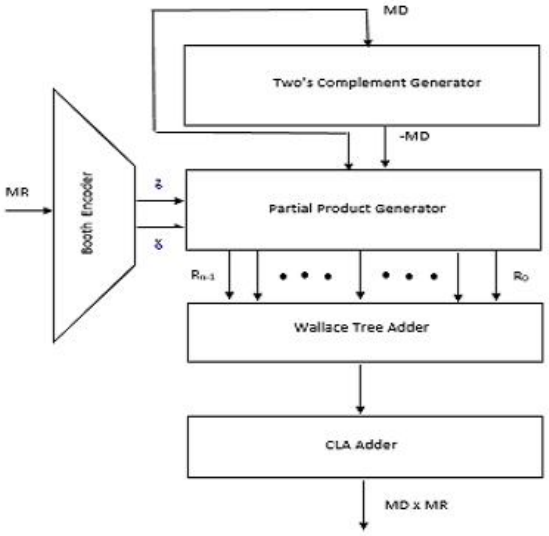

Fig. 4. Booth-encoded Wallace Tree Multiplier

V. FFT with Booth-Encoded Wallace Tree Multiplier

FFT implementation using Booth-encoded Wallace Tree Multiplier is an efficient circuit with advantages of both Booth Multiplier and Wallace Tree Multiplier. As explained in II, Modified Booth Algorithm is used to calculate Partial Products as per Table II. Partial Product Generator provides minimum number of partial products which are added using Wallace Tree structure. Hence, efficient algorithm of multiplication is implemented.

Radix-2 8-point DIT-FFT has been coded in Verilog HDL for input values scaled up by a factor of 10000. There are ten inputs to the circuit, namely, eight time-domain samples, Twiddle factor 'wr' and the scaling factor 'k'. Outputs are separately obtained for real and imaginary parts of corresponding frequency components.

VI. FFT and EEG

Virtually all sciences in the world contribute to the maintenance of human health and the practice of medicine. Medical physicists and biomedical engineers support the effective utilization of this medical science and technology

as their responsibilities to enhance human health care with the new development of the medical tools such as Electroencephalogram. Electroencephalography (EEG) is a mechanism of measuring electrical activity of the brain. Upon studying EEG signals, various health conditions can be monitored and diagnosed e.g. Brain diseases like Alzheimer, Tumors, Head injuries, Epilepsy, Dementia, Human Behaviour, etc. These signals are recorded from various positions on scalp through electrodes and conductive media. Diagnostic results are made from the spectral content of EEG signals. Here comes the importance of FFTs in EEG signal analysis. They are extensively used in neuroscience, cognitive science and cognitive psychology due to its capability to reflect both normal and abnormal electrical activity of brain .

EEG signals are typically represented either through rhythmic activity or transients. Rhythmic Activity of brain signals is divided into different bands of frequency, namely, Delta, Theta, Alpha, Beta, Gamma. Table III. shows the frequency range of each band and the different states of the person [1]. Amongst these bands, Alpha band is widely used for various diagnostic studies [8]. Real-time applications like alerting drivers about their drowsiness through EEG variations in Alpha band is one of its kind. EEG signal analysis are crucial for evaluating Epilepsy. In marketing field, EEG signals have been used to study customer response to various products in market as a feedback method and product improvement study, referred to as neuro-marketing.

In this work, EEG signal analysis is used to classify EEG levels of Autistic persons in Alpha band. Autism is a brain development disorder whose symptoms are visible since childhood. Autistic children due to seizures, show high delta and theta waveforms and low alpha waveform due to less metabolism. EEG signal pattern of normal persons are similar for similar age group, sex, race, food habits, environmental conditions, etc. However, frequency bands will remain the same for all people. Different types of special children show variations in EEG signals in Alpha band depending on their neurological function. Hence they can classified by comparing values of mid-frequency Alpha band of normal and Autistic persons.

TABLE III. FREQUENCY BANDS IN EEG SIGNAL

EEG bands	Frequency band(in Hz)	Prominent
Delta	Less than 4	Deep sleep
Theta	4-7	Drowsiness
Alpha	8-13	Relaxed and awake
Beta	14-30	Sleep stages
Gamma	>30	Finger movements

VII. Simulation Results

The proposed design has been simulated using Xilinx and Modelsim, the wave form obtained after simulating is as shown in figures

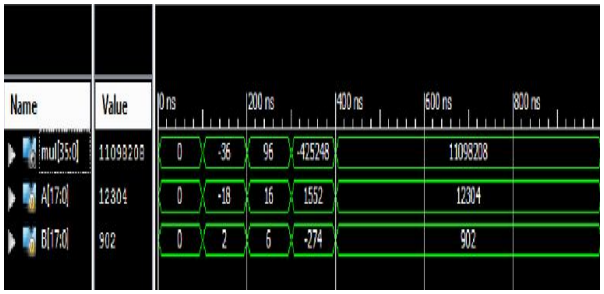

Fig. 5. Simulation Results of Booth-encoded Wallace Tree Multiplier

The RTL schematic of the proposed system is as shown in belowfig. , then it simulated result is implemented on FPGA Spartan 3E.

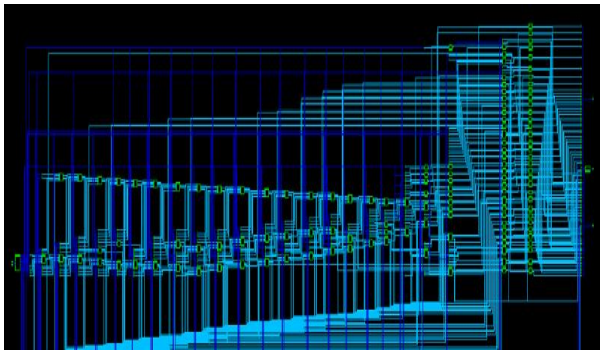

Fig. 6. Generic Gate-level Schematic of Booth-encoded Wallace Tree Multiplier

Fig. 7. Simulation Results of FFT with Booth-encoded Wallace Tree Multiplier shown in Signed Decimal Radix

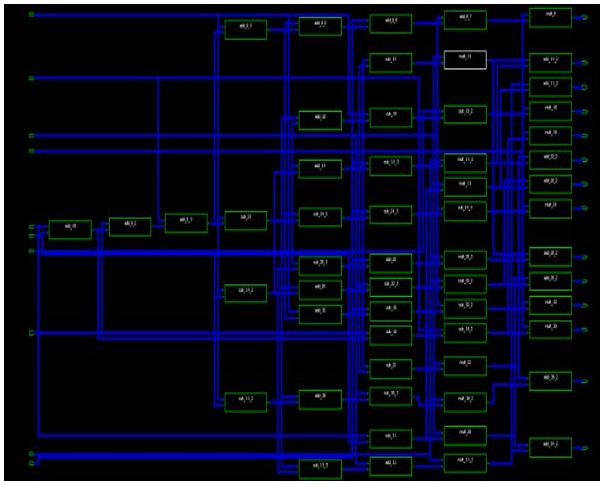

Fig. 8. Generic-Gate level Schematic of FFT with Booth-encoded Wallace Tree Multiplier

VIII. Conclusion and Future Scope

Generic-gate level implementation of Fast Fourier Transform using Booth-encoder Wallace Tree Multiplier has been done using VLSI 90nm technology. The circuit has been studied and analyzed for data accuracy and efficient performance. An accuracy of ±0.019% has been obtained for four decimal places of twiddle factor (1/ 2). On increasing the number of significant digits of the twiddle factor, accuracy of output can be improved but it will share a trade-off with the area of the circuit. Physical level chip design and further optimization of the circuit in terms of area and power and increasing the number of points for FFT computation form the future scope of work.

Autistic EEG samples can be evaluated for the midfrequency alpha band. This value is expected to be lower than normal person [1]. This circuit can thus be used to classify Autistic person based on EEG level and this work can be extended for its further analysis and verification.

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