INTERNATIONAL JOURNAL OF RESEARCH
In Advanced Engineering Technologies

Volume 5, Issue 4 OCT 2016

Implementation of Area Delay Efficient Carry Skip Adder by Using Verilog HDL

Doddi Suresh [1] **T.Swetha** [2] **B.Ramu**[3]
doddisuresh4@gmail.com[1] swetha1121@gmail.com[2] ram582018@gmail.com[3]
[1]PG Scholar, Dept of ECE, Dhruva Institute of Engineering & Technology, Toopranpet Choutuppal, Nalgonda,Telangana India.
[2]Assistant Professor, Dept of ECE, Dhruva Institute of Engineering & Technology, Toopranpet Choutuppal, Nalgonda, Telangana India.
[3]Associate Professor, HOD, Dept of ECE, Dhruva Institute of Engineering & Technology, Toopranpet Choutuppal, Nalgonda, Telangana India.

Abstract- The speed enhancement is achieved by applying concatenation and instrumentation schemes to improve the good organization of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the arrangement make use of AND-OR Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. Which lowers the power utilization without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the loose time, and hence, enable a more voltage reduction. The proposed structures are assessed by compare their velocity power, and energy parameters with those of other adders using a 45-NM static CMOS technology for a wide range of supply voltages. A carry skip adder (CSKA) structure that has a higher pace yet lower get-up-and-go consumption compared with the conventional one. A variable latency adder employs speculation the exact arithmetic function is replace with an approximated one that is faster and gives the correct result most of the time, but not always. The approximated adder is augmented with an error detection network that asserts a mistake signal when speculation fails. A story variable latency peculative adder based on HanCarlson parallel- prefix topology that resulted more helpful than variable latency Kogge-Stone topology. The paper describes the stages in which variable latency speculative prefix adders can be subdivided and presents a tale error detection network that reduce error probability compared to previous approaches. Several variable latency speculative adders, for a variety of operand lengths by means of both Han-Carlson and Kogge-Stone topology.

Key Words: Carry skip adder(CSKA),energy efficient, high performance, hybrid variable latency adders, voltage scaling

I. Introduction

Adders are a key building block of maths and logic units (ALUs) [1] and hence increasing their speed and reducing their power/energy expenditure strongly affect the speed and power consumption of processors. There are countless works on the subject of optimizing the speed and power of these units, which have been report in [2]–[9].Obviously, it is highly desirable to achieve higher speeds at low power/energy consumptions, which is a challenge for the designers of general point processors. One of the effective techniques to lesser the power consumption of digital circuits is to reduce the supply voltage due to the

quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, which is the main leakage component in OFF campaign has an exponential dependence on the supply voltage level through the drain induced barrier lowering effect [10]. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the group hold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions. In the sub threshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nano scale technologies. The variations increase uncertainties in the aforesaid performance parameters. In addition, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region [10]. ADDERS ARE basic functional units in computer sums Binary adders are used in microprocessor for addition and subtraction operations as well as for floating point multiplication and division. Therefore adders are fundamental components and improving their performance is one of the major challenges in digital designs. Theoretical do research [1] has established lower bounds on the area and delay of -bit adders: the former varies linearly with udder size, the latter has a behavior. High swiftness adders are based on well established similar prefix architectures [1], [2], including Brent-Kung [3], Kogge-Stone [4], Sklansky [5], Han-Carlson [6], Ladner-Fischer [7], Knowles [8]. These standard architectures operate with undying latency. Better average performances can be achieved by using patchy latency adders, that have been recently proposed in literature[9]. A variable latency adder employs speculation: the exact arithmetic utility is replaced with an approximated one that is faster and gives the correct result most of the time, but not always. The approximated adder is augmented with an error detection network that asserts an output gesture when speculation fails.

II. Literature Survey

On the basis of necessities such as space, delay and power consumption a number of the advanced adders square measure Ripple Carry Adder, Carry look-Ahead Adder and Carry choose Adder. Ripple Carry Adder (RCA) shows the compact style however their computation time is longer. Time essential applications build use of Carry Look-Ahead Adder (CLA) to derive quick results however it leads to increase in space. However the carry choose adder provides a compromise between tiny the tiny the little} spaces however longer delay of RCA and giant area with small delay of Carry Look Ahead adder. Ripple Carry Adder consists of cascaded “N” single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path known as worst case delay path through N stages. Fig. one shows the diagram of ripple carry adder. Currently as the price of N will increase, delay of adder can additionally increase in a linear manner. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. Now CSLA provides a way to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. Therefore the conventional CSLA makes use of Dual RCA’s to generate the partial sum and carry by considering input carry Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers.

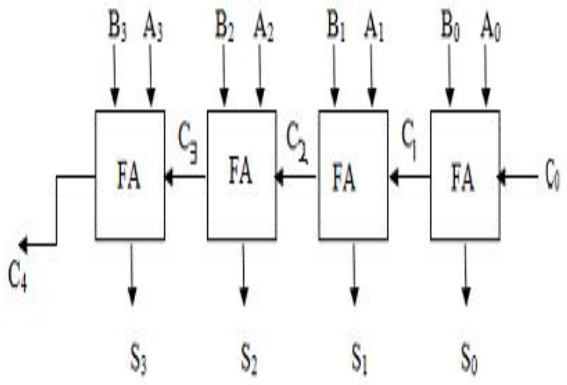


Fig. 1 4-bit Ripple Carry Adder

III. Existing System

Modifying CSKAs for Improving Speed

Alioto and Palumbo propose a simple strategy for the design of a single-level CSKA. The method is based on the VSS technique where the near-optimal numbers of the FAs are determined based on the skip time (delay of the multiplexer), and the ripple time (the time required by a carry to ripple through a FA). The goal of this method is to decrease the critical path delay by considering a non integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio. In all of the works reviewed so far, the focus was on the speed, while the power consumption and area usage of the CSKAs were not considered. Even for the speed, the delay of skip logics, which are based on multiplexers and form a large part of the adder critical path delay [19], has not been reduced.

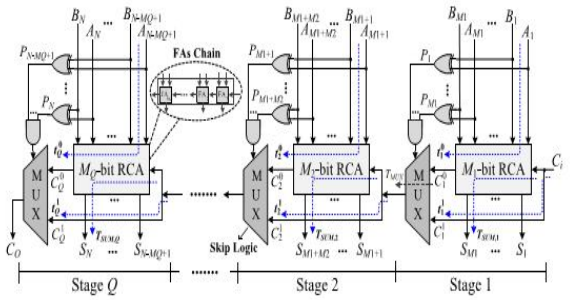


Fig. 2. Conventional structure of the CSKA

Ripple Carry Adder

The ripple carry adder structure is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the adding of the two binary digits at different stage of the ripple carry [9]. The carry out of one stage is fed directly to the carry-input to the next stage. A number of full adders circuits may be added to the ripple carry adder or ripple carry adders of the different sizes may be cascaded in the order which accommodate binary vector strings of larger sizes [7]. For an n-bit parallel adder, it requires n number of computational elements (FA). The worst-case delay of the RCA is when a carry signal propagates ripples through all the stages of adder chain from the LSB to the MSB, which is approximated by: $T = (n-1)\,tc + ts$

Where the tc is the delay through the carry stage of a different full adder, and ts is the delay used to compute the sum of the last stage.

Drawbacks:

- More area overhead system
- More power consumption
- Low speed architecture

Skip Logic

The skip logic contains the AOI (AND OR Invert) and OAI (OR AND Invert) compound

gates for skip logic. The gates, which consist of fewer transistors, havelower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer [7]. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the exisiting one. Note that while the power consumed by the AOI (or OAI) gate are smaller than that of the multiplexer, hence the power consumption of the proposed CI-CSKA is a little more than that of the conventional carry skip adder structure.

IV Proposed CSKA Structure

The structure is based on combining the concatenation and the incrementation schemes [13] with the Conv CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates (Fig. 2). The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer [37]. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

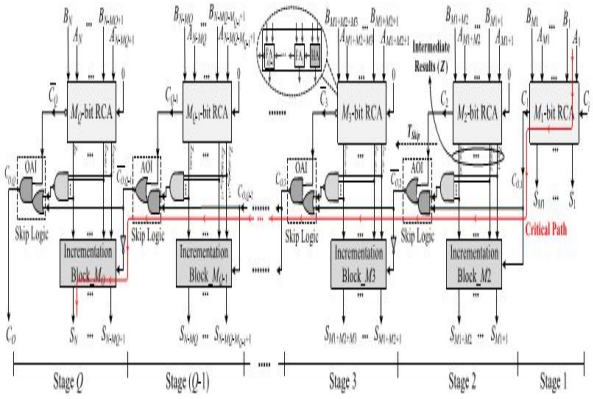


Fig. 3. Proposed CI-CSKA structure

The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries. This way the need for an inverter gate, which increases the power consumption and delay, is eliminated. As shown in Fig. 3, if an AOI is used as the skip logic, the next skip logic should use OAI gate. In addition, another point to mention is that the use of the proposed skipping structure in the Conv-CSKA structure increases the delay of the critical path considerably. This originates from the fact that, in the Conv-CSKA, the skip logic (AOI or OAI compound gates) is not able to bypass the zero carry input until the zero carry input propagates from the corresponding RCA block.

Advantages:

- Less area overhead system
- Less power consumption
- High speed architecture

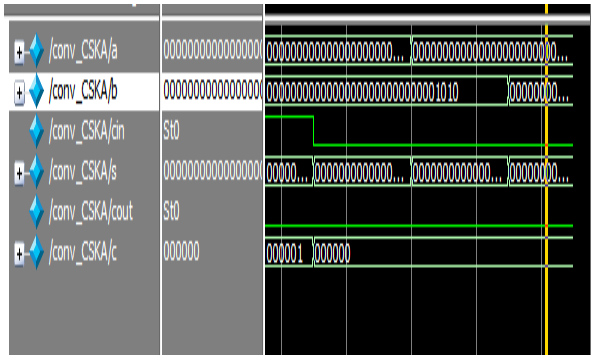
V.Results

The written Verilog HDL Modules have successfully simulated and verified using

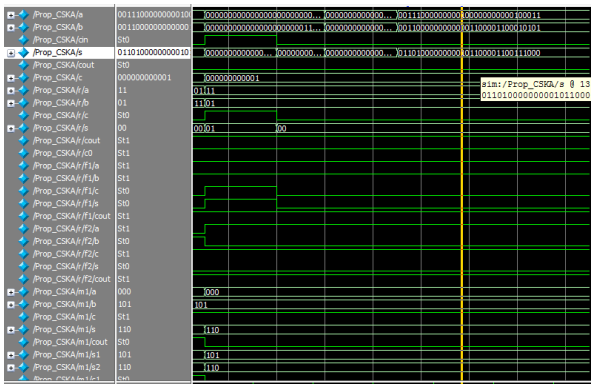
Modelsim6.4b and synthesized using Xilinxise13.2.

Simulation Results:

Conv-CSKA:

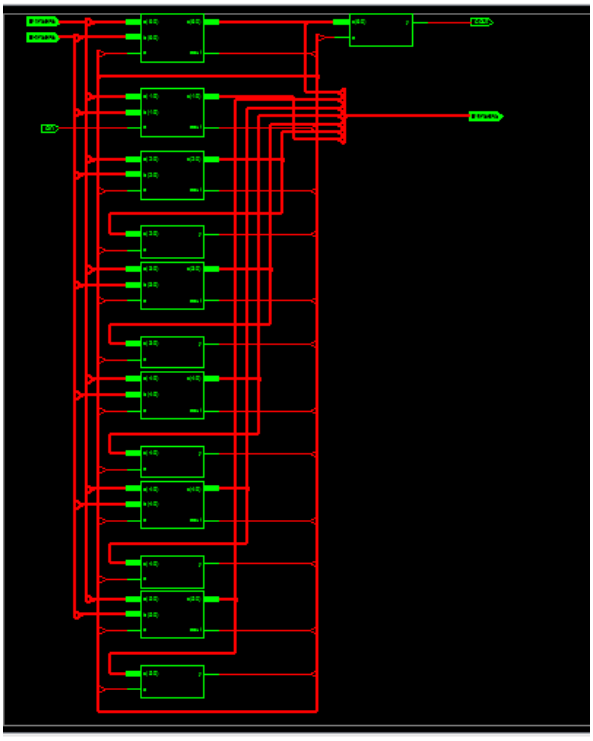


Proposed CSKA:

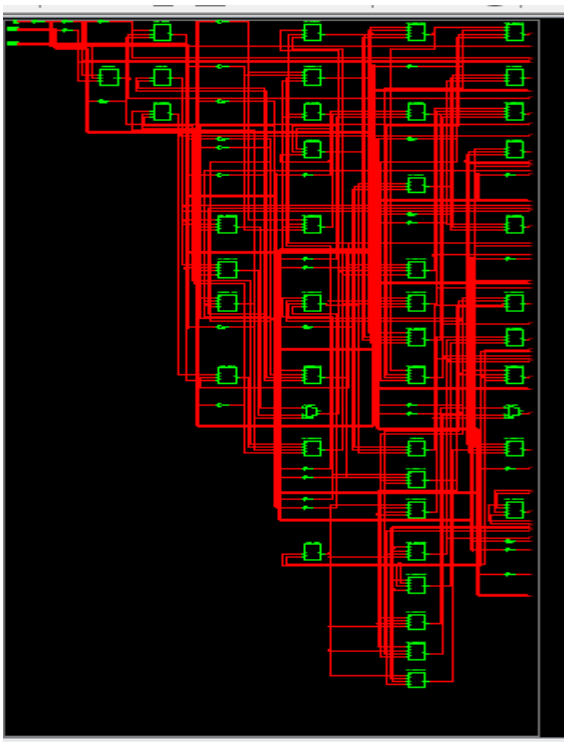


Synthesis Results:

RTL Schematic:



Technology Schematic:



Design Summary:

tjrr Project Status (09/02/2016 - 16:04:08)			
Project File:	tjrr.ise	Current State:	Synthesized
Module Name:	Prop_CSKA	• Errors:	No Errors
Target Device:	xc3s500e-4fg320	• Warnings:	No Warnings
Product Version:	ISE 10.1 - Foundation Simulator	• Routing Results:	
Design Goal:	Balanced	• Timing Constraints:	
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	

tjrr Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	70	4656	1%
Number of 4 input LUTs	122	9312	1%
Number of bonded IOBs	98	232	42%

Conclusion:

In this paper, Carry Skip Adder (CSKA) structure was proposed, which exhibits a higher speed and lower energy consumption compared with the conventional structure. The speed is through the concatenation and efficiency by the incrementation techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied. The results also suggested that the CSKA structure is a very good adder for the applications where both the speed and energy consumption are critical. In addition, a hybrid variable latency extension of the structure was proposed which reduces the power without affecting the speed of the structures.

Future Enhancement:

In our Base paper they are Implemented 8 Bit, 16 Bit, and 32 Bit Existing and Proposed adders. Now our proposed architecture converted into 128 bit Adders and analyzes the area power. This adder will be done by using our verilog and the Adder design will implemented into FPGA Spartan3E.

REFERENCES

1. Koren, Computer Arithmetic Algorithms, 2nd ed. Natick, MA, USA: A K Peters, Ltd., 2002.

2. R. Zlatanovici, S. Kao, and B. Nikolic and koren ,"Energy–delay optimization of 64-bit carry-lookaheadadders with a 240 ps 90 nm CMOS design example," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 569–583, Feb. 2009.

3. S. K. Mathew, M. A. Anders, B. Bloechel, T. Nguyen,R. K. Krishnamurthy, and S. Borkar, "A 4-GHz 300-mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS," IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 44–51, Jan. 2005.

4. V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, and R. Krishnamurthy, "Comparison of high-performance VLSI adders in the energy-delay space," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 754–758, Jun. 2005.

5. B. Ramkumar and H. M. Kittur, "Low-power and area-efficient carry select adder," IEEE Trans. Very LargeScale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 371–375, Feb. 2012.

6. M. Vratonjic, B. R. Zeydel, and V. G. Oklobdzija, "Low- and ultra low-power arithmetic units: Design and comparison," in Proc. IEEE Int. Conf. Comput. Design, VLSI Comput. Process. (ICCD), Oct. 2005, pp. 249–252.

7. C. Nagendra, M. J. Irwin, and R. M. Owens, "Area-time-power tradeoffs in parallel adders," IEEE Trans.Circuits Syst. II, Analog Digit. Signal Process., vol. 43, no. 10, pp. 689–702, Oct. 1996.

8. Y. He and C.-H. Chang, "A power-delay efficient hybrid carry- lookahead/carry-select based redundant binary to two's complement converter," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 1, pp. 336–346, Feb. 2008.

9. C.-H. Chang, J. Gu, and M. Zhang, "A review of 0.18 µm full adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.

10. D. Markovic, C. C. Wang, L. P. Alarcon, T.-T. Liu, and J. M. Rabaey, "Ultralow-power design in near-threshold
region," Proc. IEEE, vol. 98, no. 2, pp. 237–252, Feb. 2010.