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DATA ENCODING SCHEME FOR POWER REDUCTION IN NETWORK ON CHIP LINKS USING VERILOG HDL

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Abstract: Network-On-Chip (NOC) structure makes a fitting substitution for system on chip designs incorporating large number of processing cores. In network the main source of power dissipation is in the network on chip links. The dynamic power dissipation in links is major contributor to the power consumption in NOC. This effort investing sates the reduction of transition activity using gray coding schemes. Our advanced scheme does not require any change of the routers and link architecture. The future scheme uses the binary to gray conversion at the transmitter and gray to binary conversion at the receiver. An investigational result has shown the effectiveness of the proposed schemes, with respect of power dissipation and area overhead in the Network Interface (NI) as compared with data encoding.

Keywords-Binary to gray conversion, Data encoding, Interconnection on chip, Low power, Network-on-chip (NOC), Power analysis, Gray to binary conversion.

I. Introduction

The Network on chip is an emerging approach for the implementation of on chip communication architecture. The system on chip designs incorporating large no. of processing cores and modular structure of Network on chip makes a fitting replacement for system on chip. Network on chip is intended to solve the shortcomings of these, by implementing a communication network of switches, micro routers and resources. System on chips are not containing IP cores only and traditional methods for communication such as bus are not suitable solution for future System on chips. The Network-on Chip has emerged as underlying infrastructure for communication between Intellectual Property cores. Network on chip is solution for communication architecture of future System on chips that are composed of switches and IP cores where communicate among each other through switches. Between IP cores data move in the form of packet. As the technology shrinks the power ratio between link and router increase making link more power hungry than routers.

A network on chip communication gives flexibility in the topology, in support to that the flow control, Advance routing algorithms, self switching techniques guarantying the quality of service. Network on chip is an approach to design the communication subsystem between intellectual property cores in a system on chip. The communication strategy in system on chip uses dedicated buses between communicating resources. This will not give any flexibility since the needs of the communication, in each case, have to be thought of every time a design is made. Another possibility is the use of common buses, which have the problem that it does not scale very well, as the number of resources grows.

The advances in fabrication technology allow designers to implement a whole system on a single chip, but the inherent design complexity of such systems makes it hard to fully explore the technology potential. Thus, the design of Systems-on-Chip (SoCs) is usually based on the reuse of predesigned and pre-verified intellectual property core that are interconnected through special communication resources that must handle very tight performance and area constraints. In addition to those application-related constraints, deep submicron effects pose physical design challenges for long wires and global on-chip communication. A possible approach to overcome those challenges is to change from a fully synchronous design paradigm to a globally asynchronous, locally

synchronous (GALS) design paradigm. A network on-Chip (NoC) is an infrastructure essentially composed of routers interconnected by communication channels. It is suitable to support the GALS paradigm, since it provides asynchronous communication, scalability, reusability and reliability.

II. Related Work and Motivation

The accessibility of chips are growing every years. In the next several years, the availability of cores with 1000 cores is foreseen[3]. Since the focus of this paper is on reducing the power dissipated by the links, here we briefly review some of the works in the area and link power reduction. Also these include some technique. There are, use of shielding [4], [5], increasing line-to-line spacing [6], [7], and repeater insertion [8]. Thus the above all the techniques having large area overhead. Another one method is the data encoding technique it mainly fo cus on reducing the link power reduction. The data encoding technique is classified into two categories. In the first category is mainly concentrate on minimizing the power due to self-switching activity of each bus lines and avoid the power dissipation due to coupling switching activity. In this category, bus invert [BI] [9] and INC -XOR [10] have been proposed. When the random patterns are transmitted via these lines. On the other hand, gray code [11], T0 [12], working -zone encoding [13], and T0-XOR [14] have been proposed for the case of correlated data patterns.

In this first category of encoding is not suitable for applied in deep sub -micron meter technology nodes where the coupling capacitance is a main part of the total interconnects capacitance. This causes the power due to the coupling switching activity to become a large portion of the link power reduction. In the second category concentrate on reducing power dissipated through the reduction of the coupling switching [7], [14] -[15]. The technique proposed in[16], proposed a method on power effective Bus Invert. In [15] they presented a method based on Odd/Even Bus -Invert techniques. If the number of switching transitions is half of the line width means the odd inversion is performed. In [9], the number of transitions from 0 to 1 for two data packets is counted. The number of 1‘s in the data packet is larger than the half of the links means the inversion will be performed and the number of 1‘s is reduced to 0 transitions when the packets are transfer through the links. In [17], the technique is used to reducing the coupling switching. From this method, the encoder counts the Type I transitions with the weighting coefficient of one and the Type II transitions with the weighting coefficient of two. If the number of 1‘s is larger than half of the links means the inversion will be performed and it reducing the power consumption on the links. The technique proposed in [1] using the data encoding technique. This technique illustrate if the bits are encoded before they are injected into the network with the goal of minimizing the self-switching and the coupling switching in the links. These two are the main reason for the link power dissipation. Here they are classified the encoding technique into three scheme based on the four Types. In scheme 1 using the odd inversion and scheme 2 using the both odd inversion and full inversion and scheme 3 using the both odd, full and even inversion. Based on the odd, full and even inversion the power dissipation is reduced o n the Network on chip (NOC) links. In this paper we present gray encoding technique, which focused on reducing the errors during the transition from transmitter to receiver and reducing the power dissipation in the links.

III. Overview of Project

Development of technology allows designers to use an Evolution system on chips. But complexity of such systems creates a difficult to inheritance and using their properties to growth and completing them. So designing of systems on chip which is based on using of their previous properties, by correlation of resources should manage together in a common confine, introduces some challenges for physical designing and way of changing system physical architecture. A network on chips (NOC) consists of interior communication resources which have relation by channels. Rectifying switching activity in networks and also reduction of data changing in these networks were considered. For decreasing them, encoding or decoding can be used in this algorithm.

The basic idea of the proposed approach is encoding the flits before they are injected into the network with the goal of minimizing the self-switching activity and the coupling switching activity in the links traversed by the flits. In fact, self-switching activity and coupling switching activity are responsible for link power dissipation. In this paper, we refer to the end-to-end scheme. This end-to-end encoding technique takes advantage of the pipeline nature of the wormhole switching technique. Note that since the same sequence of flits passes through all the links of the routing path, the encoding decision

taken at the NI may provide the same power saving for all the links.

IV. Proposed Encoding Schemes

In this section, we present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activities on the links of the interconnection network. The datas could be classified into 4 types based on the bit transition. The data which have zero bit transition that is type 1 and one bit transition in the sense that is type 2 and two bit transition in the sense that is type 3 and more than 2 bit transition in the sense that is type 4. In this project for reduce the bit transition we are doing encoding scheme. The type 4 is encoded into type 1 and transmitted at last it is decoded and get the(type 4) original signal. And type 3 is encoded in to type 2 and its transmitted and get the original signal (type 3). There is no change on type 2 and type 1 because of the reason bit transition value is low.

The encoder and the decoder were designed in Verilog HDL described at the RTL level, synthesized with synopsys design compiler and mapped.Some of encodings reduce expenditure only when the number of bosses are high or some of encodings have high level of efficiency when the number of data transferring are many, some of methods require knowledge of static parameters and interior traffic, but we use a method that it needs no one of above, in fact we use a common method.

TYPE 1	TYPE 2	TYPE 3	TYPE 4
0000, 1111	0001, 0011 0111, 1000 1100, 1110	0010, 0100 0110, 1001 1011, 1101	0101, 1010

S.NO	NORMAL	ENCODED
1	TYPE 4	TYPE 1
	0101,1010	0000,1111
2	TYPE 3	TYPE 2
	0010,0100	0001,0011
	0110,1001	0111,1000
	1011,1101	1100,1110
3	TYPE 2	TYPE 2
	0001,0011	0001,0011
	0111,1000	0111,1000
	1100,1110	1100,1110
4	TYPE 1	TYPE 1
	0000,1111	0000,1111

Base of this method is encodings performed on Bus networks. In these methods, method of encoding by decreasing average number of signal transferring has suggested strongly. In some of these methods some parameters of interior traffic is required, but in this research has suggested strongly. In some of

these methods some parameters of interior traffic is required, but in this research we simulate a method on networks.

Which doesn't require such information. Usually in encoding methods based on possibility, there's no need to know about network traffic, they act according to statistic flow. Intelligent bit is encoded according has suggested strongly. In some of these methods some parameters of interior traffic is required, but in this research to it's past and real value and acts based on approximate statistic information.

The main goal of the proposed encoding scheme is to reduce the power dissipation by minimizing the coupling transition activities on the links of the interconnection network. In [17], they are classified four types of coupling transitions. A Type I occurs when one of the line is switches and re maining one is unchanged. A Type II occurs when one of the lines switches from low to high and another one is switches from high to low. A Type III occurs both the lines switches simultaneously. A Type IV occurs when both the lines are remains unchanged. The coupling switching activity (Tc) is defined as a weighted sum of different types of coupling transition contribution [17]. Therefore

$$Tc = K1T1 + K2T2 + K3T3 + K4T4 \qquad \text{eq. (1}$$

Where Ti is the average number of Type I transition and Ki is the corresponding weight.

A. Gray code:

The gray code is also knows as reflected binary code. It is a binary numeral system, where two successive values differ in only one bit. The reflected binary code was originally designed to prevent false output from electromagnetic switches. It is mainly used for error correction application in digital communications.

B. Problem with binary code:

The problem with binary codes is that, with real switches. The switches will change states exactly in synchronously. In binary code, the two successive values differ in one or more bits. if the output pass through a sequential system then the sequential system may store a false value. The gray code solves the above problem by changing only one bit at a time.

Decimal	Binary Code (input)	Gray Code (output)
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

Table 1: Binary to Gray converter

C. Scheme I:

In scheme 1, our main goal is to reducing the number of Type 1 transitions and Type 2 transitions. Type 1 transitions is converted into Type III and Type IV transitions and Type II transitions is converted into Type I transitions. This scheme compares the two data‘s based on to reducing the link power reduction by doing odd inversion or no inversion operation.

Time	Normal			Odd inverted			Even inverted		
	Type 1			Type II, III, IV			Type II,III, and IV		
t – 1	00,11	00,11,01,10	01,10	00,11	00,11,01,10	01,10	01,10	00,11,01,10	00,11
t	10,01	01,10,00,11	11,00	11,00	00,11,01,10	10,01	10,01	00,11,01,10	11,00
	T1'	T1''	T1'''	Type iii	Type IV	Type II	TypeII	Type IV	Type iii
t-1	Type II			Type I			Type I		
t	01,10			01,10			01,10		
	10,01			11,00			00,11		
t-1	Type II			Type II			Type I		
t	00,11			00,11			00,11		
	11,00			10,01			01,10		
t-1	Type II			Type II			Type II		
t	00,11,01,10			00,11,01,10			00,11,01,10		
	00,11,01,10			01,10,00,11			10,01,11,00		

Table 2: Effect of Odd and Even inversion on change of Transition Types

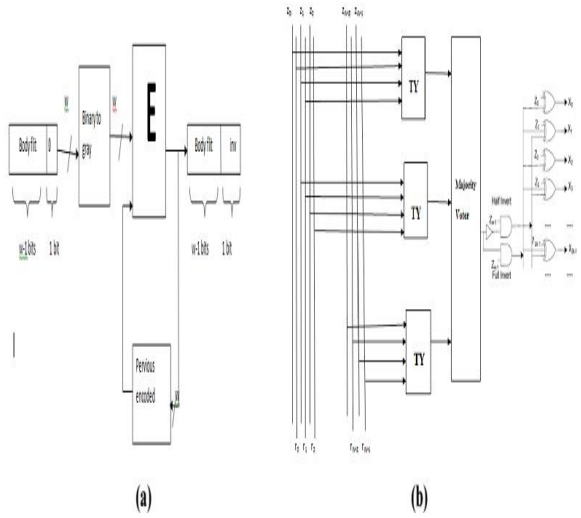

Fig.1.Scheme1.(a)Block diagram. (b) Architecture for encoder block

Ty > Tx eq. (2)

Ty > 0.5 (w-1) eq. (3)

The general block diagram in Fig. 1(a) is same for scheme 1, scheme 2 and scheme 3. The w-1 bit is given to the one input of the binary to gray conversion block. This block converts the original binary input into gray output. The output of the gray code is given as input of encoder block and another input of the encoder block is the previously encoded output. The encoder block compares these two inputs and performing the any one of the inversion based on the transition types. The block E is vary for all the three schemes. Comparing the current data and previous encoded data to decide which inversion is performed for link power reduction. Here the TY block this takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs, whether more number of type 1 and type 2 transitions is occurring means it set the output state to 1, otherwise it set the output to 0. The odd inversion is performed for these type of transitions.Then the next block is the Majority code it checks the state, if the number of one‘s is greater than zeros or not and it implemented using a simple circuit. The last stage using the XOR circuits, these circuit is used to perform the inversion on odd bits. The decoding is performed by simply inverts the encoder circuit when the inverting bit is high.

D. Scheme II:

In scheme II, our main goal is to reducing the number of Type II transitions. Type II transitions are converted into Type IV transitions. This scheme compares the two data‘s based on to reducing the link power reduction by doing full inversion or odd inversion or no inversion operation.

T2 > T4** eq. (4)

Full and odd inversion based this advanced encoding architecture consist of w-1 link width and one bit for inversion bit which indicate if the bit travel through the link is inverted or not. W bits link width is considered when there is no encoding is applied for the input bits. Here the TY block from scheme 1 is added in scheme 2. This takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs. We have T2 and T4**blocks which determines if any of the transition types T2 and T4**occur based on the link power reduction. The number of ones blocks in the next stage. The output of the TY, T2 and T4** send through the number of one‘s blocks. The output of the ones block is log 2w. The first ones block is used to determine the number of transitions based on odd inversion. The second ones block determines the number of transitions based on the full inversion and the then another one ones block is used to determine the number of transitions based on the full inversion. These inversions are performed based on the link power reduction. Based on these ones block the Module A takes the decision of which inversion should be performed for the link power reduction. For this module is satisfied means the output is set to _1‘. None of the output is set to _1‘ if there is no inversion is takes place. The module A is implemented using full adder and comparator circuit.

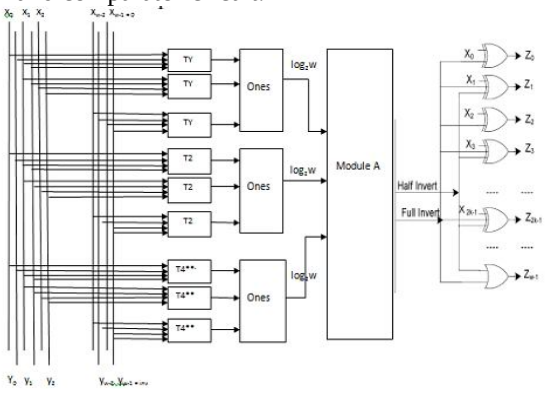

Fig.2. Encoder architecture scheme II

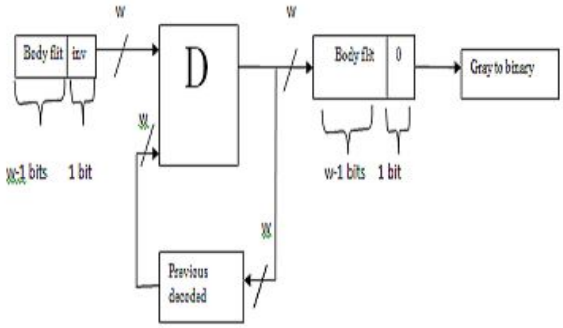

Fig.3. Block diagram for decoder

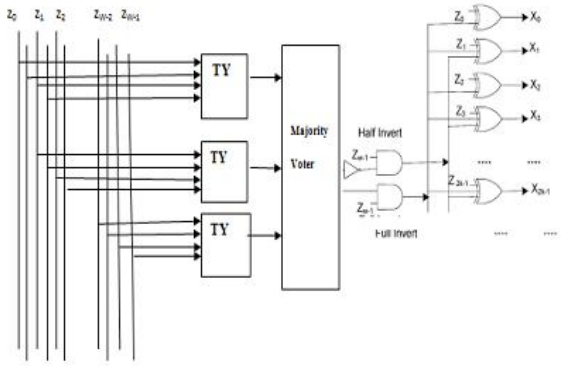

Fig.4. Decoder architecture scheme II

The block diagram of the decoder is shown in Fig.3. The w-1 bits input is applied in the decoder circuit and another input of the decoder is previous decoded output. The decoder block compares the two input data‘s and inversion operation is performed and w-1 bits output is produced. The remaining one bit is used to indicate the inversion is performed or not. Then the decoder output is given to the gray to binary block. This block co nverts the gray code into original binary input. In decoder circuit diagram (Fig.4.) consist of TY block and Majority vector and Xor circuits. Base d on the encoder action the TY block is determined the transitions. Based on the transitions types the majority blocks checks the validity of the inequality given by(2). The output of the majority voter is given to the Xor circuit. Half inversion, full inversion and no inversion is performed based on the logic gates.

E. Scheme III:

In scheme III, we are adding the even inversion into scheme II. Because the odd inversion converts Type I transitions into Type II transitions. From table II, T 1**/T1*** are converted into Type IV/Type III transitions by the flits is even inverted. The link power reduction in even inversion is larger than the Odd inversion.

The encoding architecture (Fig.5) in scheme III is same of encoder architecture in scheme I and II . Here we adding the Te block to the scheme II. This is based on even invert condition, Full invert condition and Odd invert condition. It consist of w-1 link width input and the w bit is used for the inversion bit. The full, half and even Inversion is performed means the inversion bit is set _1‘, otherwise it set as _0‘.The TY, Te and T4** block determines the transition types T2, Te and T4**. The transition types are send to the number of ones block. The Te block is determined if any of the detected transition of types T 2, T1** and T1**. The ones block determines the number of ones in the corresponding transmissions of TY, T2, Te and T4**. These number of ones is given to the Module C block. This block check if odd, even, full or no invert action corresponding to the outputs _10‘, _01‘, _11‘ or _00‘ respectively, should be performed. The decoder architecture of scheme II and scheme III are same.

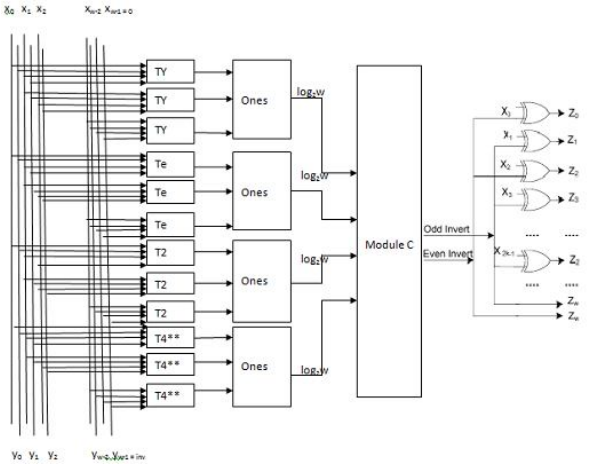

Fig.5. Encoder architecture for scheme III

V. Results and Discussion

Fig.6. shows the simulation result of scheme I (reducing Type I and Type II transitions) using gray encoding technique. The output of the scheme I reducing the number of Type I and Type II transitions by using the odd invert condition. Fig.7. shows the simulation result of scheme II (convert Type II transitions into Type IV) using gray encoding techniques. In scheme II the number of type II transition is converted into Type IV transitions by using the odd and full inversion condition.

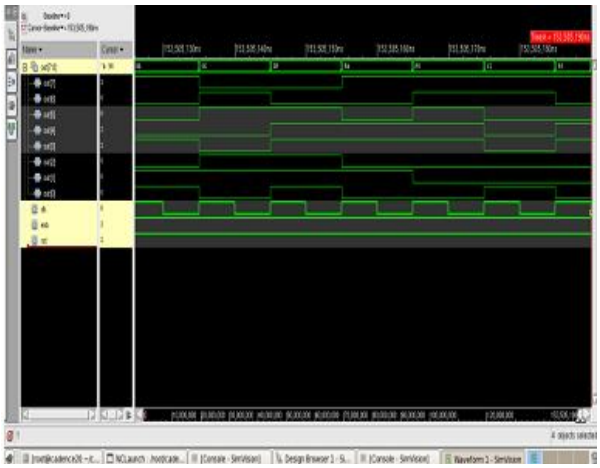

Fig.6. Simulation for scheme I using gray encoding

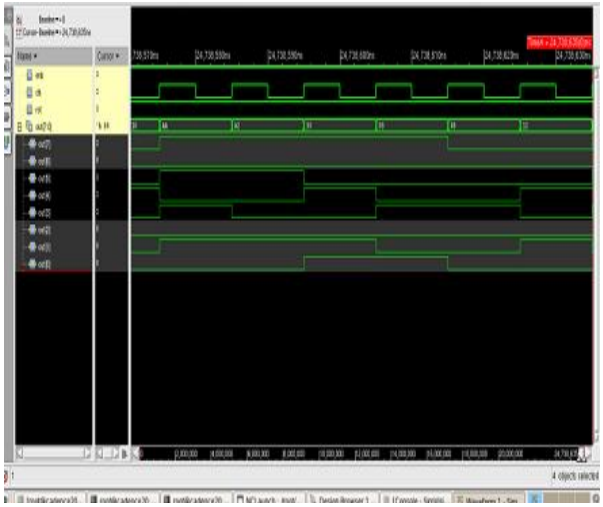

Fig.7. Simulation for scheme II using gray encoding

Fig.8. shows the simulation result of scheme III(Type I (T1***) converted into Type II) using the gray encoding. The output of the scheme III reducing the number of Type I (T 1***) into Type II transitions by using odd, full and even inversion.

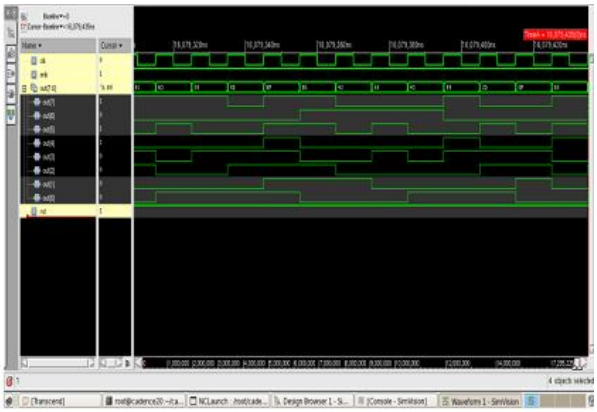

Fig.8. Simulation for scheme III using gray encoding

VI. Conclusion and Future Work

In this work, the gray encoding technique is implemented for reducing the transition activity in the NOC. This gray encoding scheme aimed at reducing the power dissipated by the links of an NOC. In fact links are responsible for
a significant fraction of the overall power dissipated by the communication system. The proposed encoding schemes are agnostic with respect to the underlying NOC architecture in the sense that our application does not require any modification neither in the links nor in the links. The proposed architecture is coded using VERILOG language and is simulated and synthesized using cadence software. Overall, the application scheme allows savings up to 42% of power dissipation and with less than 5% area overhead in the NI compared to the data encoding scheme.

In the future, the Network On Chip (NOC) implementation using different types of router technique will be analyzed. Comparison on many encoding techniques such as gray encoding techniques will be analyzed in which the area, delay, power and the performance of the NOC will be investigated and use for high speed applications.

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