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Design and Implementation of Reconfigurable FIR Filter using VHBCSE Algorithm

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Abstract- Design of efficient hardware architecture for fixed point FIR filter has been considered. In FIR filter, the multiplication operation is performed between one particular variable and many constants and known as the multiple constant multiplications (MCM). The algorithms proposed earlier to implement this MCM for an efficient FIR filter design can be categorized in two main groups:1) graph based algorithms and 2) common sub-expression elimination algorithms (CSE). A CSE algorithm using binary representation of coefficients for the implementation of higher order FIR filter with a fewer number of adders than Canonic Signed Digit (CSD)-based CSE methods is used In this system we used vertical-horizontal binary common sub-expression elimination (VHBCSE) algorithm states that to manipulate the 16 bit input by layered operation. A 2-bit vertical BCSE has been applied first on the adjacent coefficient, followed by 4-bit and 8-bit horizontal binary common sub expressions elimination to detect and eliminate which are present within each of the coefficient. Thus there will be a power consumption by minimum switching activity. The partial products generated by VHBCSE method and controlled additions are used by using any efficient adder to produce output efficiently. Further elimination of the common sub expressions has been performed through finding the common sub expressions present within the coefficients by applying BCSE algorithm of different lengths horizontally to different layers of the shift and add based constant multiplier architecture reconfigurable fir filter designed using VHBCSE algorithm based constant multiplier establishes the suitability of the proposed algorithm for efficient fixed point reconfigurable FIR filter synthesis .

Keywords: common sub expression sharing, multiple constant multiplications, genetic algorithm.

I. Introduction

Recent advances in mobile computing and communication applications demand low power and high speed VLSI Digital Signal Processing (DSP) systems. One of the most important operations in DSP is finite impulse response filtering. The FIR filter performs the weighted summations of input sequences and is widely used in mobile communication systems for variety of tasks such as channelization, channel equalization, pulse shaping and matched filtering due to their properties of linear phase and absolute stability. The digital filters employed in mobile systems must be higher order and realized to consume less power and operate at high speed. Recently evolving as a promising technology in the area of wireless communications is Software Defined Radio (SDR). The idea behind SDR is to replace most of the analog signal processing in the transceivers with digital signal processing in order to provide the advantage of flexibility through reconfiguration or reprogramming. This will support multistandard wireless communications in different air-interfaces to be implemented on a single hardware platform. SDR receiver must be realizing of low power consumption and high speed. The most

computationally demanding block of a SDR receiver is channelizer which operates at the highest sampling rate. Channel filter which extracts multiple narrowband channels from a wideband signal using a bank of FIR filter. In polyphase filter structure, decimation can be done to channel filtering so that need to operate only low sampling rates. The speed of operation of the channel filter is reduced by using polyphase filter structure. The aim of the wireless communication receiver is to realize its applications in mobile, low area and low power is possible by implementation of FIR channel filter.

Channelizer requires high speed, low power and reconfigurable FIR filters. The problem of designing FIR filters is dominated by a large number of multiplications, which increases area and power even if implemented in full custom integrated circuits. The multiplications are reduced by replacing them into addition, subtraction and shifting operation. The main complexity of FIR filters is dominated by the number of adders/subtractors used to implement the coefficient multipliers. To reduce the complexity, the coefficient can be expressed in common subexpression elimination methods based on Canonical Signed Digit (CSD) representation to minimize the number of adders/subtractors required in each coefficient multiplier. The aim of CSE algorithm is to identify multiple occurrences of identical bit patterns present in coefficients, to eliminate the redundant multiplications. The proposed CSE method which improved adder reductions and low complexity FIR filter compared to the existing implementation. The reconfigurability of FIR filter depends on Reconfigurable Multiplier Block (ReMB). The ReMB, which generate all the coefficient products and multiplexer which select the required coefficient depends on the inputs. This multiplexer used to reduce the redundancy in the multiplier block design [6]. In wireless communication application reconfigurable filters are meet adjacent channel attenuation specification. In this paper, to propose two architectures that integrates reconfigurability and low complexity. The architectures are Constant Shift Method (CSM) and Programmable Shifts Method (PSM). Multiplication of single variable (input signal) with multiple constants (coefficients) is known as Multiple Constant Multiplications (MCM) [8]. The MCM is optimized for eliminating redundancy using proposed CSE algorithm to minimize the complexity.

II. Existing System

The existing system based on 2 and 3 bit BCSE algorithm that expresses multiplying the input (X) and the coefficient (H) partial products are generated and each bit is allowed through 4:1 multiplexers and addition shift operation takes place. The several adders are used to add the generated multiplexers output. At final a 2:1 multiplexer used to generates the 16 bit output. Choice of the BCS of fixed length (3-bit or 2-bit) in the earlier proposed BCSE algorithm based reconfigurable FIR filter designs leaves a scope to optimize the designed filter by considering the BCS across the adjacent coefficients as well as within a single coefficient. 2-bit BCSE algorithm is a method of assigning the values that existing in the sequence by leaving the upcoming two bits of each bit. 3-bit BCSE algorithm is a method of assigning the values that existing in the sequence by leaving the upcoming three bits of each bit. The convention considered for representing the input and the coefficient of the earlier designed FIR filter has signed magnitude format also gives a scope to modify the data representation to signed decimal number for wider applicability of the proposed FIR filter in any systems. On studying the above-mentioned literatures, it has been realized that the

development of an efficient reconfigurable constant multiplier is very much needed for its applicability in any reconfigurable system.

III. Literature Review

Memory-Based Realization of FIR Digital Filter by Look-Up-Table Optimization.

Finite impulse response (FIR) digital filter is widely used in signal processing and image processing applications. Distributed arithmetic (DA)-based computation is popular for its potential for efficient memory-based implementation of finite impulse response (FIR) filter where the filter outputs are computed as inner-product of input-sample vectors and filter-coefficient vector. In this paper, however ,we show that the look-up-table(LUT)-multiplier-based approach, where the memory elements store all the possible values of products of the filter coefficients could be an area-efficient alternative to DA based design of FIR filter with the same throughput of implementation. Finite-impulse-response (FIR) filters are basic processing elements in applications such as video signal processing and audio signal processing. The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop-band. Many applications in digital communication

Design and Analysis of Multiplier less Finite Impulse Response Filter.

It is well known that if the individual multiplier coefficients in a digital filter can be expressed as a sum of powers-of-two, then the digital filter can be implemented in hardware without any need for actual digital multipliers. Since the multiplier is the circuit module occupying the largest silicon area, and is also the slowest, filters without multipliers are not only economical in silicon area but also fast. The improvements in speed and savings in silicon area are, however, achieved at the expense of deterioration in the frequency response characteristics. The extent to which the frequency response deteriorates depends on the number of power -of-two terms used in approximating each coefficient value, the architecture of the filter, and the discrete space optimization technique used to derive the coefficient values. There are several methods available for the optimization of FIR filters with powers-of-two multiplier coefficients by using local search algorithms. Among these methods, the Mixed Integer Linear Programming (MILP) optimization technique has become extremely popular. This optimization technique guarantees global optimality in the Min/Max sense, but is limited in scope to the design of linear phase FIR filters with the number of multiplier coefficients less than about 40. But the local search techniques have been found to perform.

A Low Complexity Reconfigurable Non-uniform Filter Bank for Channelization in Multi-standard Wireless Communication Receivers.

In a typical multi-standard wireless communication receiver, the channelizer must have the capability of extracting multiple channels (frequency bands) of distinct bandwidths corresponding to different communication standards. The channelizer operates at the highest sampling rate in the digital front end of receiver and hence power efficient low complex architecture is required for cost effective implementation of channelizer. Re configurability is another key requirement in the channelizer to support different communication standards. In this paper, we propose a low complexity reconfigurable filter bank (FB) channelizer

based on coefficient decimation, interpolation and frequency masking techniques. The proposed FB architecture is capable of extracting channels of distinct (non-uniform) bandwidths from the wideband input signal. Design example shows that the proposed FB offers multiplier complexity reduction of 83% over Per-Channel (PC) approach and 60% over Modulated Perfect Reconstruction.

IV. Proposed System

Vertical and horizontal BCSEs are the two types of BCSE used for eliminating the BCSs present across the adjacent coefficients and within the coefficients respectively in any BCSE method. Vertical BCSE produces more effective BCS elimination than the horizontal BCSE. However, this paper proposes one new BCSE algorithm which is a combination of vertical and horizontal BCSE for designing an efficient reconfigurable FIR filter. By using this proposed algorithm number of multiplexer used will be less. multiplier switching activities get reduced in our proposed algorithm, a 2-bit vertical BCSE has been applied first on the adjacent coefficient, followed by 4-bit and 8-bit horizontal BCSEs to detect and eliminate as many BCSs as possible which are present within each of the coefficient.

VHBCSE ALGORITHM

A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. It is built using binary adders. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of partial products, and then summing the partial products together. This process is similar to the method taught to primary schoolchildren for conducting long multiplication on base-10 integers, but has been modified here for application to a base-2 (binary) numeral system. Older multiplier architectures employed a shifter and accumulator to sum each partial product, often one partial product per cycle, trading off speed for die area. Modern multiplier architectures use the Baugh–Wooley algorithm, Wallace trees, or Dadda multipliers to add the partial products together in a single cycle. Here this multiplier architecture uses VHBCSE algorithm. The performance of the Wallace tree implementation is sometimes improved by modified Booth encoding one of the two multiplicands, which reduces the number of partial products that must be summed.

Data flow diagram

The details of the blocks in the fig-1 is explained here Sign Conversion Block: Sign conversion block is needed to support the signed decimal format data representation for both the input and the coefficient. The architecture of the sign conversion block is shown in Fig. 6. There is one 1's complement circuit to generate the inverted version of the 16-bit (excluding MSB) coefficient. One 16-bit 2:1 multiplexer produces the multiplexed coefficients depending on the value of the most significant bit (MSB) of the coefficient. For negative value of the original coefficient, the multiplexed coefficient will be in the inverted form; otherwise it will be as it is.

Multiplexers Unit: The multiplexer unit is used to select the appropriate data generated from the PPG unit depending on the coefficient's binary value. At layer-1, eight 4:1 multiplexers are required to produce the partial products according to the 2-bit BCSE algorithm applied vertically on the Multiplier Adder Tree (MAT). The widths of these 8 multiplexers are 17, 15, 13, 11, 9, 7, 5, and 3-bit each instead of 16-bit for

all, which would reduce the hardware and power consumption.

Control Logic (CL) Generator: Control logic generator block takes the multiplexed coefficient (Hm[15:0]) as its input and groups it into one of 4-bit each (Hm[15:12], Hm[11:8], Hm[7:4], and Hm[3:0]) and another of 8-bit each (Hm [15:8], Hm[7:0]).The CL generator block will produce 7 control signals depending on the equality check for 7 different cases. The architecture for the control signal generator block is shown in Fig. 8. The control signal for 8-bit equality check is seen to be produced through the control signals generated from the 4-bit equality check.

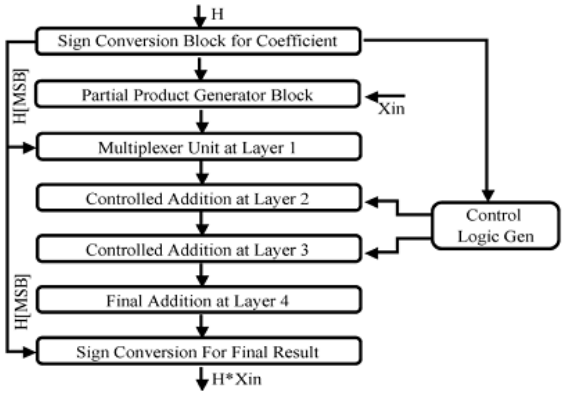

Fig-1: Data flow diagram of multiplier using VHBCSE algorithm

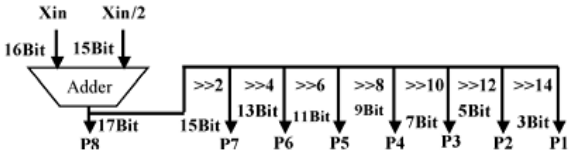

Fig -2: (Module 1) Partial product generator.

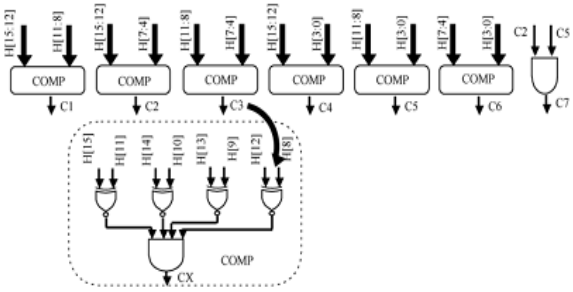

Fig-3: control logic generator unit.

Partial Product Generator (PPG): In BCSE method, shift and add based technique has been used to generate the partial product which will be summed up in the following steps/layers for producing the final multiplication result. Choice of the size of the BCS defines the number of partial products. In the proposed algorithm in the layer-1, 2-bit binary common sub-expressions (BCSs) ranging from "00" to "11" have been considered, which will produce 4 partial products. But, within four of these BCSs, a single adder (A0) will be required to generate the partial product only for the pattern "11"; the rest will be generated by hardwired shifting. For the coefficient of 16-bit length,8 partial products of 17, 15, 13, 11, 9, 7, 5, and 3 bits (P8-P1) will be generated by right shifting the first partial product (P8) by 0, 2, 4, 6, 8, 10, 12, and 14 bits respectively. This technique helps in reducing the multiplexer's size which is used next to select the proper partial product depending on the coefficient's binary value.

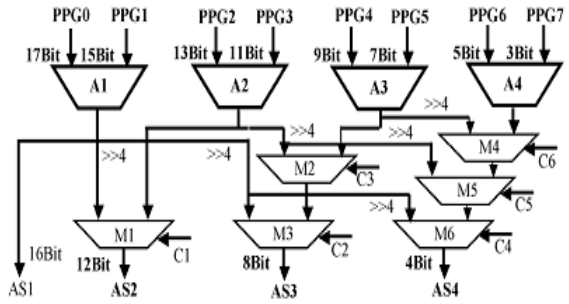

Fig. 4. Architectural details of the controlled addition at layer-2 block.

Controlled Addition at Layer-2:The partial products (PP) generated from eight groups of 2-bit BCSs are added up for the final multiplication results which have been performed in three layers. According to the BCSE algorithm [14] proposed earlier, layer-2 requires four addition (A1-A4) operations to sum up the eight PPs. Instead of direct addition of these PPs, the controlled addition operations are performed at layer 2 according to the proposed VHBCSE algorithm. These adders (A1-A4) are controlled depending on the control signals (C1-C6), which were generated based on 4-bit BCSE from the control signal generator block. The architecture of this block is shown in Fig. 4, which reveals that the propagation delay will be the maximum between the paths which has been used to generate AS2, AS3, AS4.

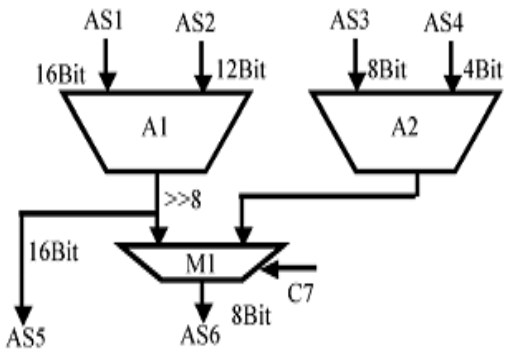

Fig. 5. Hardware architecture of the controlled addition at layer-3.

Controlled Addition at Layer-3: The four multiplexed sums (AS1, AS2, AS3 and AS4) generated from layer-2 are now summed up in layer-3. In our algorithm, controlled additions are performed, instead of direct addition of these four sums as shown in Fig.5. Hence, this addition (A6) is controlled by the control signal (C7) which has been generated based on 8-bit BCSE from the CS generator block

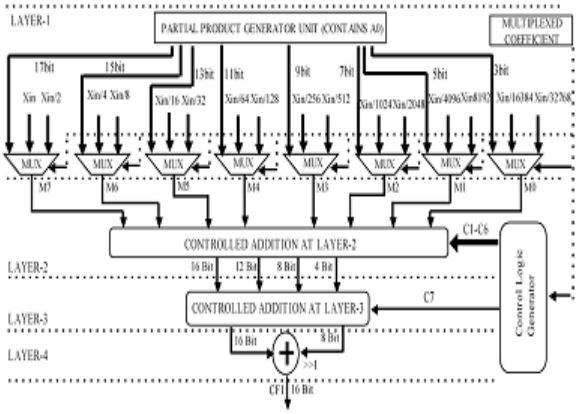

Fig. 6. Proposed Reconfigurable constant multiplier architecture

Final Addition on Layer-4:This block performs the addition operation between the two sums (AS5-AS6) produced by layer-3 to finally produce the multiplication result between the input and the coefficient. The block diagram of the over-all constant multiplication is shown in Fig. 6.

CONCLUSIONS

A view to design an efficient FIR filter, new vertical horizontal BCSE algorithm is used, which removes the initial common sub-expressions by applying BCSE vertically. By using this algorithm, there will be maximization in efficiency of the multiplier.

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