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PERFORMANCE ANALYSIS OF THREE-LEVEL BACK-TO-BACK VSC-HVDCSYSTEM USING SPACE VECTOR MODULATION UNDER FAULTS CONDITIONS

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ABSTRACT- A comprehensive model of the Back-to-Back HVDC system based on the three-level Diode Clamped converter is proposed in this paper. The ac-side controllers are achieved in a synchronous rotating reference frame (d-q) controls direct and quadrature currents to obtain independent control of real and reactive powers. Here the controlling is achieved by using the PI controller. By using the space vector modulation the balancing control of the DC capacitor of the back to back connected VSC is achieved with balancing strategy based on the effective use of the redundant switching states of the inverter voltage vectors. The proposed methods demonstrate a satisfactory response of the VSC of HVDC system under various conditions of studied different normal and fault cases. The simulation results are shown in MATLAB/SIMULINK.

Key words: VSC-HVDC, Back-to-Back, multilevel space vector modulation, capacitors voltages balancing, fault conditions.

I.INTRODUCTION

HVDC transmission is well known as being advantageous for long distance, bulk power delivery, asynchronous interconnections and long submarine cable crossings. 2 basic categories of converters are thought of in HVDC technologies. There are line commutated Current source Converters (CSC) and self-commutated Voltage source Converters (VSC). the primary cluster is known because the classic or conventional HVDC system. High Voltage Direct Current (HVDC) technology has characteristics that make it particularly attractive for certain transmission applications. This family of the HVDC systems could be a mature technology that is mainly thyristor based. it's even the technology of the choice for very high power applications (~ one GW) and has been with success applied for various HVDC systems.

However, there are some disadvantages related to the line commutated thyristor converters such as (a) requirement of reactive power supply and harmonic filters at every terminal, (b) problem of commutation failure at inverters and (c) problems due to adverse system interactions with weak AC system (corresponding to low short circuit ratio (SCR) at the converter bus). VSC based HVDC systems are self-commutated with semiconductor switches like string of IGBTs in series. The emerging technology of self-commutated Voltage source converter has the benefits of overcoming these issues. The VSC based HVDC technology created a modest starting in 1997. The VSC has the benefits of independent control of active power and reactive power within the possible region in PQ diagram. Additionally they are capable of operative at higher frequencies, presently implemented for switching frequency of around 1800 Hertz. Also there is no demand of quick communication between the rectifier and inverter station for management functions. The only constraint is posed by the constraints on the IGBT and GCT devices (with turn-off capability), that square measure utilized in VSC. The need to fulfill high voltage levels, each at AC and DC sides, of an HVDC device station is best accommodated by structure VSC configurations.

They were investigated with the necessity of quality and efficiency in high power systems. They provide several advantages equivalent to increased power rating, reduced the harmonic effects and reduced electromagnetic interference (EMI) emission. Recently, HVDC convertor systems using full Back-to-Back multilevel NPC converters are being investigated attributable to their high-voltage, high-current and staircase-like wave capabilities. Pulse width modulation (PWM) techniques are showing quality to control multilevel inverters for multi-megawatt industrial applications. Space vector modulation (SVM) is one of the most popular PWM techniquesgainedinterest recently.

The salient features of the SVM strategy are as follows. i) It minimizes total harmonic distortion of the ac-side voltages, through utilization of all

available voltage levels of the VSC. ii) It minimizes the switch losses since, over every sampling amount of the SVM modulator, it uses the 3 adjacent switch states with minimum ON– OFF state transitions ofthe switch devices. iii) It allows development of a way for dc-capacitor voltage equalization while not the requirement for auxiliary power circuits and/or offline calculations. Aim of this paper is to investigate the dynamic performance of 3 levels VSC-HVDC System link using area vector pulse breadth modulation for management the each VSCs units, with equalization strategy based on the effective use of the redundant switch states of the converters voltage vectors. This paper conjointly gives a dynamic model of a three levels VSC-based HVDC converter station to design the dc-link transformer and power exchange controllers. The analysis is completed by the dynamic response under different normal and fault cases.

I. THREE-LEVELS VSC-HVDC SYSTEM STRUCTURE ANDMATHEMATICAL MODEL

Fig.1 shows a schematic representation of a three-level VSC-based HVDC system. Currently, the Back-to-Back HVDC system is considered and seen as a single device, hence the two sides support the DC link.

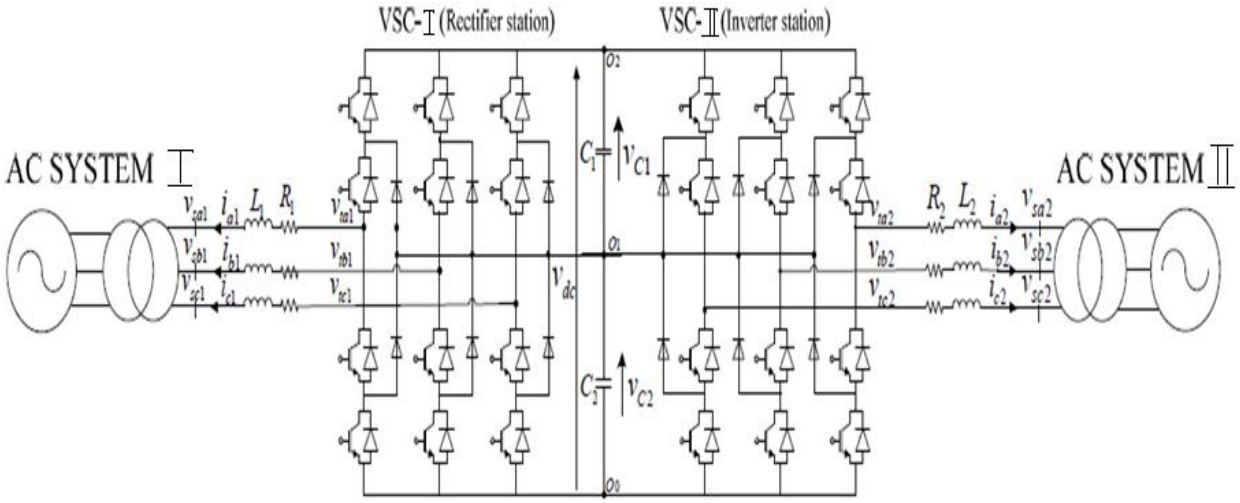

Fig 1: Three phase Back to Back three level NPC based VSC –HVDC system

The system includes two consecutive connected three level NPC converter units. The DC-link consists of two nominally-identical capacitors. The two VSC units share the same DC-capacitors and intermediate nodes O_1 are common between VSC-I and VSC-II.

An estimate of the total switching losses of the system is modeled by resistance R_p.

The AC-side terminal of every convertor is connected to the corresponding AC system through a series connected R and L and a three-phase transformer. For simplicity and without the loss of generality, we assume the following: i) the voltage magnitudes of each grids are the same; but, the phases will assume any values. ii) The power switches, diodes and passive parts of the two VSCs are correspondingly identical. To avoid repetitions within the formulation, the quantities of VSC-1 and AC system-1 are indexed by k=1, whereas those of VSC-2 and AC system-2 are indexed by k=2. In this paper, station 1 is designated and chosen as rectifier station whereas station 2 is selected as inverter station.

A. System mathematical model in abc Frame

Based on the simplified equivalent circuit of Fig. 1, the mathematical equations which govern dynamic behavior of the AC-side voltages are

$$v_{tak} = R_k i_{ak} + L_k \frac{di_{ak}}{dt} + v_{ask}$$

$$v_{tbk} = R_k i_{bk} + L_k \frac{di_{bk}}{dt} + v_{bsk}$$

$$v_{tck} = R_k i_{ck} + L_k \frac{di_{ck}}{dt} + v_{csk} \quad (1)$$

The VSCs terminal voltages defining by:

$$\begin{bmatrix} v_{tak} \\ v_{tbk} \\ v_{tck} \end{bmatrix} = \frac{1}{\sqrt{3}} m_k V_{dc} \begin{bmatrix} \sin(\theta_k) \\ \sin\left(\theta_k - \frac{2\pi}{3}\right) \\ \sin\left(\theta_k + \frac{2\pi}{3}\right) \end{bmatrix} (2)$$

Where:$\theta_k = \omega_t t + \alpha_k . m_k$and $\alpha_k$are, respectively, modulation index and phase-angle of the modulating waveforms of VSC-k. $\omega_k$is the angular frequency of AC system-k.

For the DC-link circuit, the DC-bus voltage dynamics can be described by

$$C_{eq} \frac{dv_{dcj}}{dt} = -\frac{1}{R_p} v_{dc} - (i_{dc1} + i_{dc2}) (3)$$

Where C_{eq}= C/2 and is the equivalent capacitor seen by each VSC. Based on the power balance equation of eachVSC, we deduce:

$$i_{dck} = \frac{1}{v_{dc}} (v_{tak} i_{ak} + v_{tbk} i_{bk} + v_{tck} i_{ck}) \quad (4)$$

Substituting forv_{tak},$v_{tbk}$and $v_{tck}$by their fundamentalfrequency components from (2) in (4), we deduce

$$i_{dck} = \frac{1}{\sqrt{3}} m_k \left(i_{ak} \sin(\theta_k) + i_{bk} \sin\left(\theta_k - \frac{2\pi}{3}\right) + i_{ck} \sin\left(\theta_k + \frac{2\pi}{3}\right) \right) \quad (5)$$

Equations (1) and (3) in conjunction with equations (2) and (5) represent a fundamental-frequency model of the HVDC system in abcframe[9-10].

B. System model in dq Frame

The AC System-k variables are transferred to a dqframe by[9]

$$f_{dqk} = K_k f_{abck} \quad (6)$$

Transformation matrixK_k is

$$K_k = \frac{2}{3} \begin{bmatrix} \cos(\theta_k) & \cos\left(\theta_k - \frac{2\pi}{3}\right) & \cos\left(\theta_k + \frac{2\pi}{3}\right) \\ \sin(\theta_k) & \sin\left(\theta_k - \frac{2\pi}{3}\right) & \sin\left(\theta_k + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (7)$$

Transforming variables of AC System-k, as given by (1) and (2), based on (6), we deduce

$$\begin{cases} v_{tdk} = R_k i_{dk} + L_k \frac{di_{dk}}{dt} - L_k \omega_k i_{dk} + v_{dsk} \\ v_{tqk} = R_k i_{dk} + L_k \frac{di_{dk}}{dt} + L_k \omega_k i_{qk} + v_{qsk} \end{cases} (8)$$

In (8), i_{dk}andi_{qk} are the d and q current components of AC System-k, and $v_{tdk}$and $v_{tqk}$are given by :

$$\begin{cases} v_{tdk} = \frac{1}{\sqrt{3}} m_k v_{dc} \cos(\alpha_k) \\ v_{tqk} = \frac{1}{\sqrt{3}} m_k v_{dc} \sin(\alpha_k) \end{cases} (9)$$

Where $m_k$and $\alpha_k$are

$$\alpha_k = \tan^{-1}\left[\frac{v_{tqk}}{v_{tdk}}\right],$$

$$m_k = \frac{\sqrt{3}\sqrt{v_{tdk}^2 + v_{tqk}^2}}{v_{dc}} (10)$$

Substituting for $i_{abck}$from (6) in(5), we deduce

$$i_{dck} = \frac{3}{2\sqrt{3}} m_k \left(i_{qk} \sin(\alpha_k) + i_{dk} \cos(\alpha_k) \right) (11)$$

Substituting for $i_{dck}$from (11) in (3) yields

$$C_{eq} \frac{dv_{dc}}{dt} = -\frac{1}{R_p} v_{dc} - \frac{3}{2} m_1 \left(i_{q1} \sin(\alpha_1) + i_{d1} \cos(\alpha_1) \right) - \frac{3}{2} m_2 \left(i_{q2} \sin(\alpha_2) + i_{d2} \cos(\alpha_2) \right)$$

(12)

Equations (8) and (12) represent a dqmodel of the HVDC system that is used for design of the DC- and AC-side controllers [9-10].

II. CONTROLLERS STRUCTURE FOR VSC-HVDC

The controls of a VSC-HVDC system is basically the control of the transfer of energy with independent control of active and reactive power and also keep the DC link voltage at the desired level to support the required active and reactive power commands.

C. AC-side current control

Modulation index and phase angle of the modulating waveform are the control parameters

of each VSC unite of dand q components of the terminal voltage of VSCs units, based on are decoupled through the following change of variables

$$\begin{cases} v_{tdk} = u_{dk} - L_k\omega_k i_{qk} + v_{dsk} \\ v_{tqk} = u_{qk} + L_k\omega_k i_{dk} + v_{qsk} \end{cases} \quad (13)$$

$u_{dk}$and $u_{qk}$are new control signals that are generated by two independent PI-controllers.

The d-axis PI controller is defined by

$$u_{dk} = K_{ipk}e_{dk} + K_{iik}\int_0^t e_{dk}\,dt \quad (14)$$

Where $e_{dk} = i_{dredk} - i_{dk}$

The q-axis current controller is designed in similar manner.

D. DC-Bus Voltage Control

To controlv_{dc} , we use (12). Multiplying both sides of (12) by $(C_{eq}v_{dc})$ yields:

$$\frac{d\left(\frac{1}{2}C_{eq}v_{dc}^2\right)}{dt} = -\frac{v_{dc}^2}{R_p} - \frac{3}{2\sqrt{3}}v_{dc}m_1\left(i_{q1}\sin(\alpha_1) + i_{d1}\cos(\alpha_1)\right) - \frac{3}{2\sqrt{3}}v_{dc}m_2\left(i_{q2}\sin(\alpha_2) + i_{d2}\cos(\alpha_2)\right) \quad (15)$$

Substituting for $v_{tdk}$and $v_{tdk}$from (9), into (15), we obtain

$$\frac{d\left(\frac{1}{2}C_{eq}v_{dc}^2\right)}{dt} = -\frac{v_{dc}^2}{R_p} - \frac{3}{2}\left(v_{td1}i_{d1} + v_{tq1}i_{q1}\right) - \frac{3}{2}\left(v_{td2}i_{d2} + v_{tq2}i_{q2}\right) \quad (16)$$

The left side of (16) is the rate of energy variations in$\frac{v_{dc}^2}{R_p}$ is the power dissipation in Rp. Terms$\frac{3}{2}\left(v_{td1}i_{d1} + v_{tq1}i_{q1}\right)$and $\frac{3}{2}\left(v_{td2}i_{d2} + v_{tq2}i_{q2}\right)$in (16) represent the instantaneous outgoing powers at the AC-side terminals of VSC-1 and VSC-2, respectively.

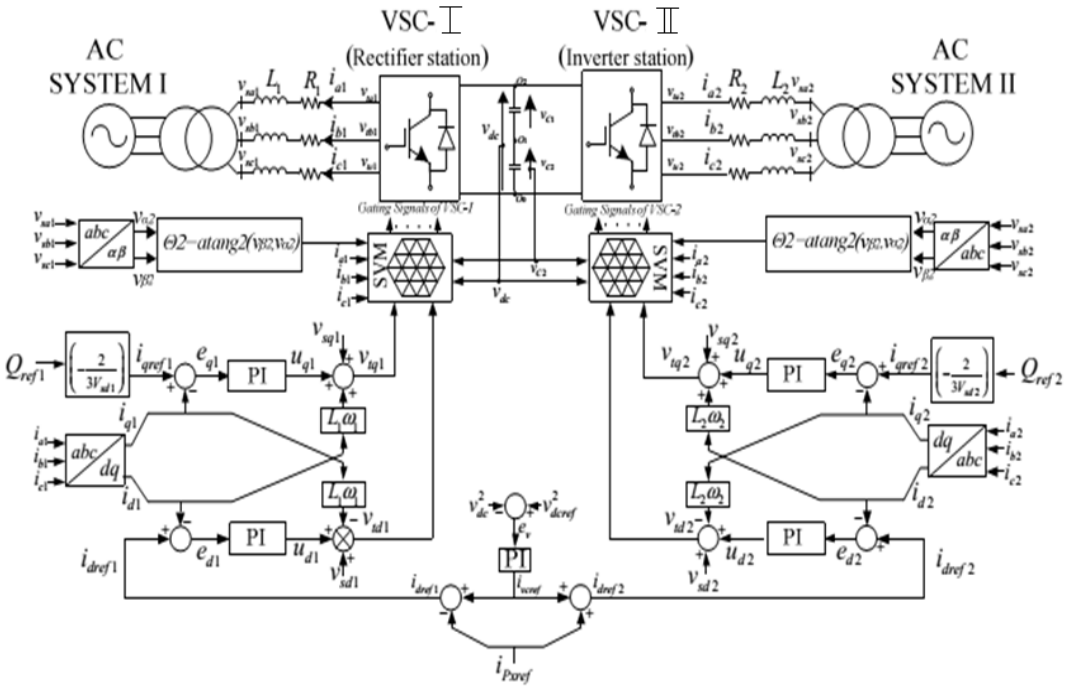

Fig:2: Control structure of the three level VSC-HVDC system

III. THREE-LEVEL SPACE VECTOR MODULATION

A three-level converter differs from a traditional two level converter in that it's capable of producing three totally different levels of output section voltage, With 3 attainable output states for each of the 3 phases, there are a complete of 27 possible switch combinations. The results of plotting every of the output voltages during a αβ organization is shown in Fig. 3. Fig.4 shows that the twenty seven switch combinations end in a complete of 19 distinctive voltage vectors since a number of the combinations produce the same voltage vector.

These different combinations relate to other ways of connecting the VSCs to the DC bus that result in an equivalent voltage being applied to AC systems. Projection of the vectors on a αβ coordinates forms a two-layer hexagon centered at the origin of the αβ plane. Zero voltage vectors area unit situated at the origin of the plane. The switch states area unit illustrated by 0 1 and 2 that denote corresponding switch states.

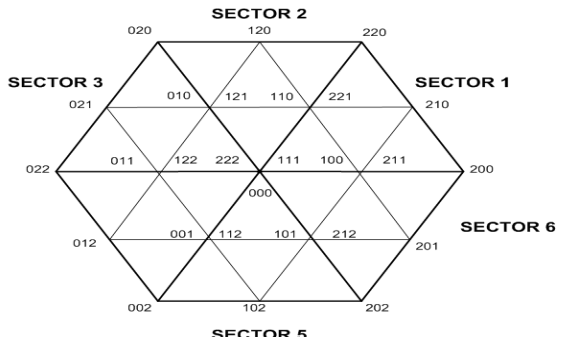

Fig 3. Space vector diagram of three-level converter

Any sampling instant the tip of the voltage vector is found during a triangle formed by three switch vectors nearest to the voltage vector (Fig. 3). The nearest 3 vectors area unit chosen by crucial Triangle inside the vector house within which the specified voltage vector resides. The specified on period of every of the vectors is decided by Equations (17). These specify that the demand vector, v_{ref} , is that the geometric add of the chosen 3 vectors (v1, v2, v3) increased by their on-durations (d1, d2, d3) which their on- durations must fill the whole cycle.

$$\begin{cases} v_1 d_1 + v_2 d_2 + v_3 d_3 = v_{ref} T \\ d_1 + d_2 + d_3 = T \\ v_{ref} = |v_{ref}| e^{j\theta}, \theta = \angle v_{ref} \end{cases} \quad (17)$$

The next step is to identify the appropriate redundant switching states and generate the switching pattern to control voltages of the capacitors. This requires knowledge of phase currents and impacts of different switching states on dc-side intermediate branch currents and consequently capacitor voltages.

V. DC-CAPACITOR VOLTAGES BALANCING STRATEGY

In a three-phase three-level VSC converter, the total energy E of DC-link capacitors is:

$$E = \frac{C}{2}(v_{c1}^2 + v_{c2}^2) \quad (18)$$

When all capacitor voltages are balanced, the total energy E reaches its minimum of $E_{min} = \frac{C_{v_{dc}^2}}{4}$.This condition is called the minimum energy property which can be used as the basic principle for dc-capacitor voltage balancing and control. The adopted control method should minimize the quadratic cost function J associated with voltage deviation of the DC-capacitors.

$$\boldsymbol{J = \frac{C}{2}(\Delta v_{c1}^2 + \Delta v_{c2}^2)} \quad \textbf{(19)}$$

VI. SIMULATION ANALYSIS AND RESULTS

To evaluate the performance of the overall HVDC system of Fig. 1 with the parameters presented in table 1, including power and control subsystems, under various dynamic operating scenarios, and the proposed SVM technique with DC-capacitor voltage-balancing strategy, a numeric simulations were carried out using the presented models implemented in MATLAB™/SIMULINK software. The system was simulated during 2.0 s.

A. Real and reactive power control

Initially, the system is in a standby mode of operation and v_{dcref} is set to 30 kV. Both VSCsunits operate at unity power factor. At t = 0.07 s up to 0.7 s, p_{ref2} is changed as a step corresponding to a power change from 0 to 10 Mw, from AC system-1 to AC System-2. At t = 0.7 s, P_{ref2} is ramped from 10 Mw to -10 Mw; this change corresponds to a power flow reversal from 10 Mw to -10 Mw, from AC system-2 to AC system-1. At t = 0.5 s, reactive power demands of AC systems 1 are changed from 0 to -5 *Mvar* and from 0 to -3 *Mvar* for AC System-2.

Fig. 4.a shows the DC voltage response, we can observe that the DC-bus voltage is maintained close to its reference with good approximation, stability and without overshoot, it is important also to note that the application of the proposed redundant vectors based three-level SVM control maintains capacitors voltages balanced to their references of $v_{dc}/2$. Figs. 4.b and 4.c shows dynamic response of the system under various steps changes in real and reactive power demands of the HVDC system. We can show that real and reactive power of AC system 1 and AC system 2 after a short overshooting are regulated at the corresponding references, and are well decoupled from each other.

Nominal net DC voltage	30KV
Resistance R_p	1.8KΩ
VSC-1 sampling frequency	2520Hz
VSC-2 sampling frequency	2520Hz
DC-link Capacitor C_1, C_2	2000μF

Simulation Parameters

Parameters of study system	Value
Each DCC nominal power	110MW
Each AC system nominal voltage	138KV
Nominal Frequencies f_1	60Hz
Nominal Frequencies f_2	50Hz
Each transformer voltage ratio	138/30KV
R_1 and R_2	40mΩ
L_1 and L_2	6mH

B. Control system performance during faults

Short-circuit faults in the grid are likely the most severe disturbance for the VSC- HVDC link. The resulting voltage dips at the converter terminals will severely hamper the ability of the link to transfer power. This may even lead to tripping of the link. At 1.2s,a single-phase-to-ground fault (Unbalance Fault) is made in phase a at the rectifier side, which drops the AC bus voltage on the faulted phase to ground during the time interval 1.2 s to 1.3 s. As shown in Fig 4.b, the voltages at inverter side (shown in Fig 4.c) are not affected by the unbalanced voltage at the rectifier side. The voltage in the faulted phase a at rectifier side is dropped to 100 V during the fault and the other two phases have maximum value is about 18 kV during the fault. At inverter side the phase currents in the faulted phase A is increased about 300A from 500 A to 800 A. in this case. The corresponding active power at inverter side is reduced during the fault, but the reactive power at inverter side does not change. The DC side voltage is well controlled except for the transient caused by the fault.

A three-phase-to-ground fault (balanced Fault) is applied at rectifier side at 1.6 s and is cleared at 5 cycles after the fault. The AC voltage at inverter side is maintained to 15 kV except small oscillations during the fault. The AC voltage at rectifier side is decreased to 1kV during the fault and recovers fast and successfully to the reference voltage after clearing the fault. The real power flow is reduced to very low value during the fault.

The DC voltage during the fault has some oscillations at the beginning of the fault and at clearing the fault, and its maximum transient value is about 3.03 kV. So the operation of the VSC-HVDC is

as expected. On the other hand, the phase currents atrectifier side decrease to low values to reduce the power flow. The phase currents at inverter side increase from 200 A to 350 A, and have overcurrent transient at the beginning of the fault.

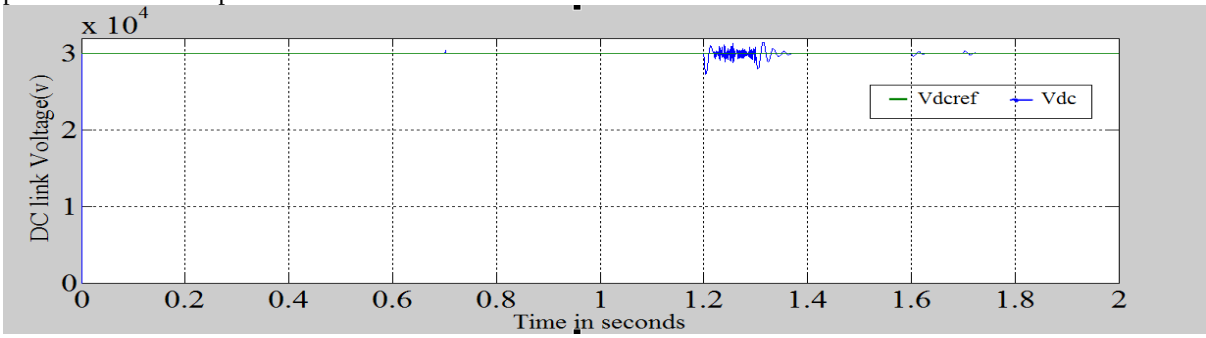

Fig:4(a): DC link voltage

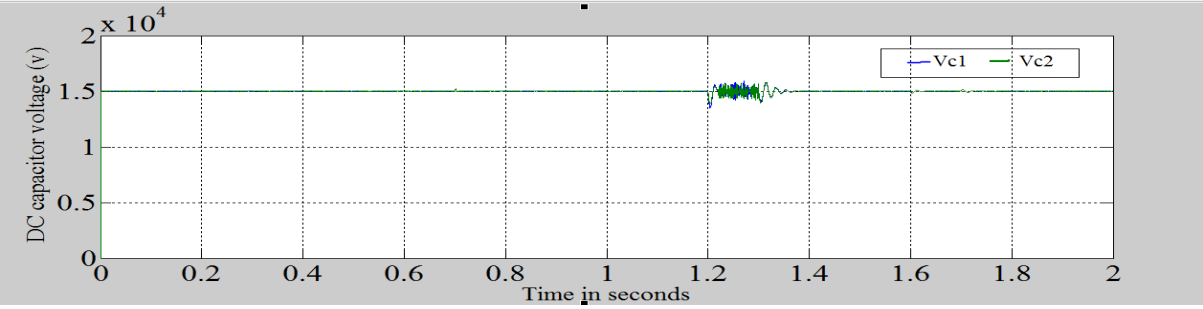

Fig:4(b): Dc voltage (v) vs Time in sec

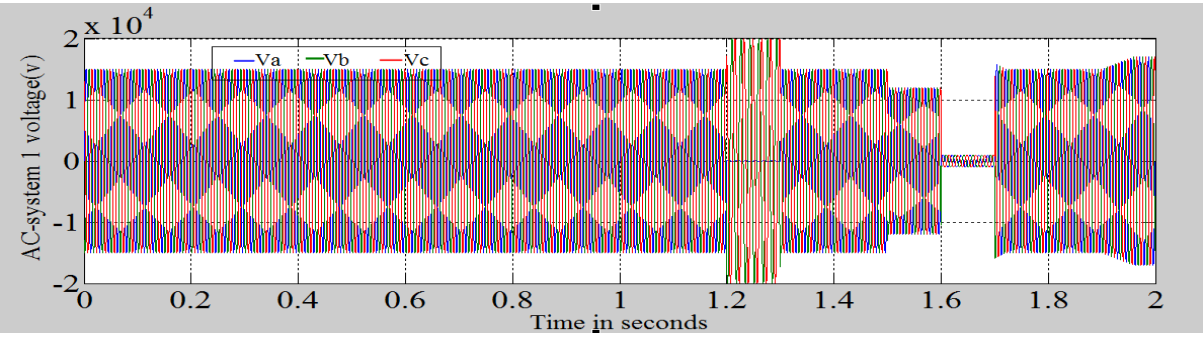

Fig :4(c)Voltage (v) of AC-system 1 vs time in sec

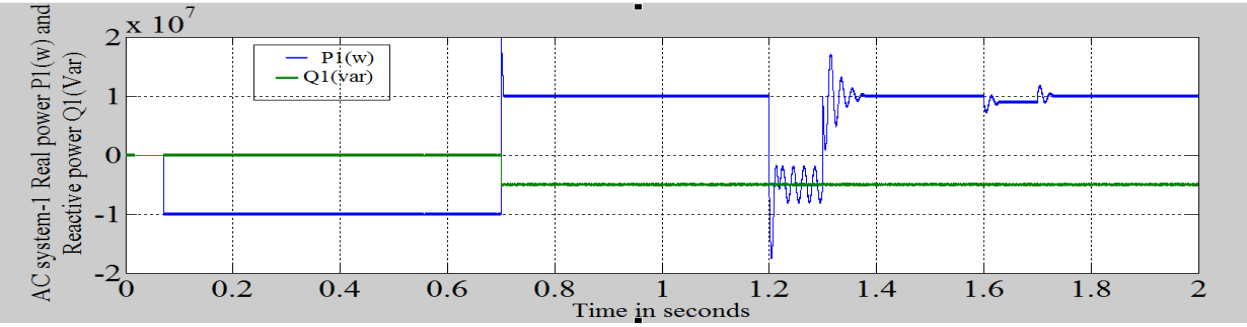

Fig :4(d)Real power(w) and Reactive power (var) of AC-system 1 vs time in sec

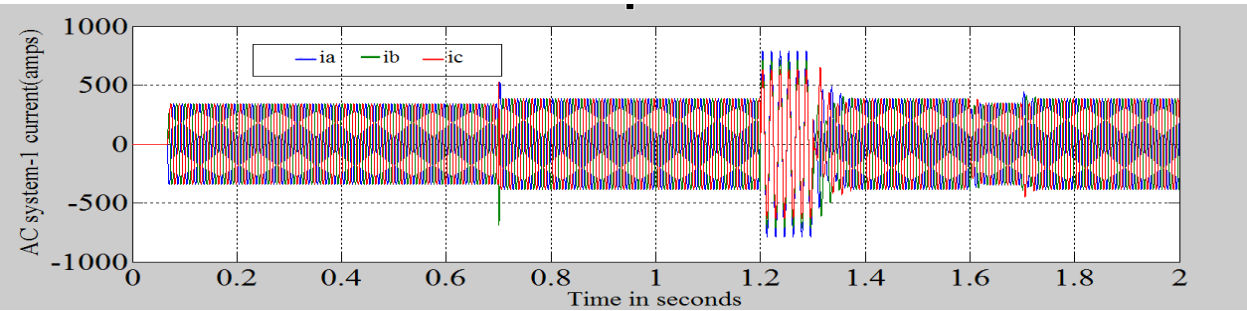

Fig :4(e)Current(amps) of AC-system 1 vs time in sec

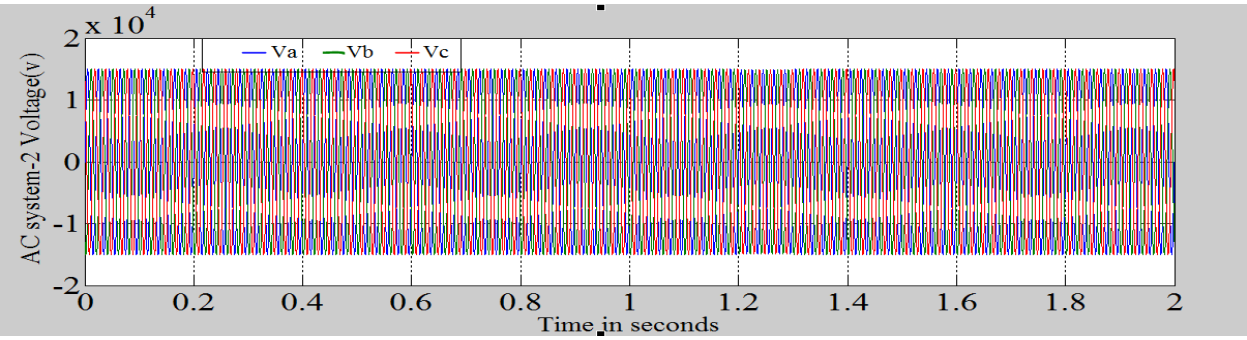

Fig :4(f)Voltage (v) of AC-system 2 vs time in sec

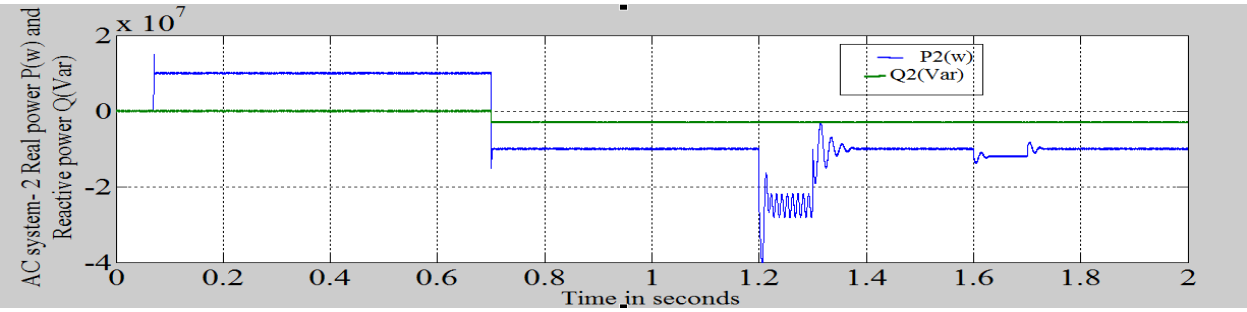

Fig :4(g) Real power(w) and Reactive power(var) of AC-system 2 vs time in sec

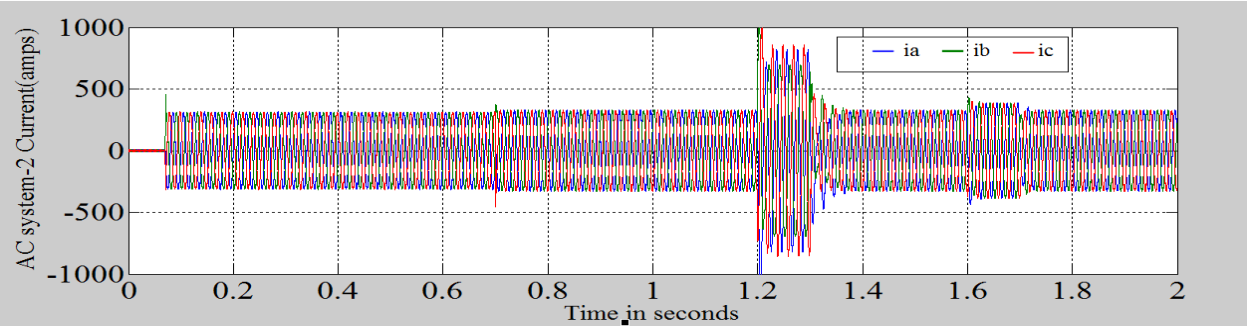

Fig 4(h)Current(amps) of AC-system -2 vs time in sec

Fig. 4. - Dynamic response of VSC-HVDC system to a step changes in active/reactive power demands and system performance under faults condition.

VII. CONCLUSION

In this paper we proposed a Back-to-Back HVDC system based on the three-level Neutral Point Diode Clamped (NPC) converter based on the space vector modulation control in both balanced and unbalanced fault conditions. The capability of the voltage balancing SVM strategy, performance of the

designed controllers, and also the overall performance of the HVDC system are analyzed based on time-domain simulation studies, in the MATLAB/SIMULINK environment. There by the split DC link voltage is maintained balanced by controlling .The studies conclude that the DC voltage balancing strategy prevents the voltage drift phenomenon of the DC-link capacitors of the HVDC system, even for the worst case scenario. The simulation results are also shown which shows the high performance of the system.

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