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Area and Power Efficient Design of Fixed Width Replica Redundancy Block Based on ANT Multiplier

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Abstract: In this paper, we have a tendency to propose a reliable low-power number style by adopting recursive noise tolerant (ANT) design with the fixed-width number to make the reduced preciseness duplicate redundancy block (RPR). The planned hymenopteran design will meet the demand of high preciseness, low power consumption, and space potency. we have a tendency to style the fixed-width RPR with error compensation circuit via analyzing of chance and statistics. Victimization the partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexness of error compensation circuit may be simplified. in an exceedingly 12×12 bit hymenopteran number, circuit space in our fixed-width RPR may be down by forty four.55% and power consumption in our hymenopteran style may be saved by twenty third as compared with the state-of-art hymenopteran style.

I.INTRODUCTION

The ascent of transportable and wireless computing systems in recent years drives the requirement for ultralow power systems. To lower the facility dissipation, offer voltage scaling is wide used as an efficient low-power technique since the facility consumption in CMOS circuits is proportional to the sq. of offer voltage. However, in deep-sub micrometer process technologies, noise interference issues have raised problem to style the reliable and economical electronics systems; thus, the planning techniques to reinforce noise tolerance are wide developed. associate aggressive low-power technique, brought up as voltage over scaling (VOS), was projected in to lower offer voltage on the far side vital offer voltage while not sacrificing the output. However, VOS ends up in severe degradation in signal-to-noise (SNR). a completely unique recursive noise tolerant (ANT) technique combined VOS main block with reduced-precision reproduction (RPR), that combats soft errors effectively whereas achieving vital energy saving. Some hymenopteran deformation styles area unit given in and therefore the hymenopterans style conception is more extended to system level.

However, the RPR styles within the hymenopterous insect styles of ar designed in a very customized manner, that aren't simply adopted and perennial. The RPR styles within the hymenopterous insect style will operate in a very in no time manner, however their hardware complexness is simply too advanced. As a result, the RPR style within the hymenopterous insect style of remains the foremost common style due to its simplicity. However, adopting with RPR in

ought to still pay further space overhead and power consumption. In this paper, we have a tendency to additional projected a straightforward means victimization the fixed-width RPR to switch the full-width RPR block. victimization the fixed-width RPR, the computation error will be corrected with lower power consumption and lower space overhead. we have a tendency to take use of chance, statistics, and partial product weight analysis to seek out the approximate compensation vector for a a lot of precise RPR style. so as to not increase the crucial path delay, we have a tendency to prohibit the compensation circuit in RPR should not be set within the crucial path. As a result, we will notice the hymenopterous insect style with smaller circuit space, lower power consumption, and lower crucial provide voltage.

II. Existing System

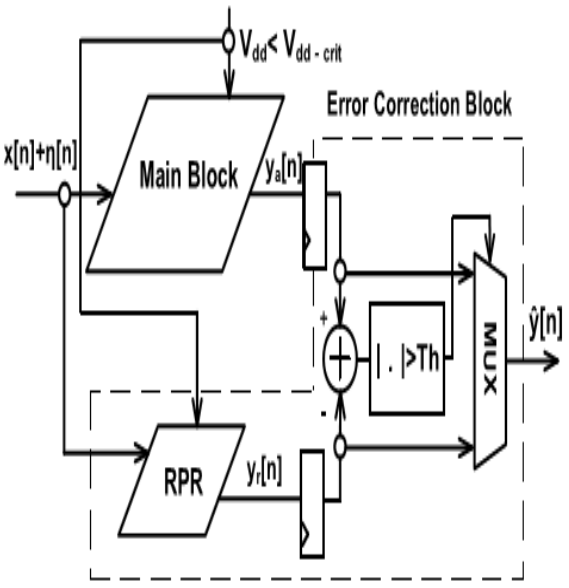

Fig.1. ANT architecture

The ANT technique includes both main digital signal processor (MDSP) and error correction (EC) block, as shown in Fig. 1. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay *T*cp of the system becomes greater than the sampling period *T*samp, the soft errors will occur. It leads to severe degradation in signal precision. In the ANT technique, a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input-dependent soft errors in its output *ya*[*n*]; however, RPR output *yr*[*n*] is still correct since the critical path delay of the replica is smaller than *T*samp. Therefore, *yr*[*n*] is applied to detect errors in the MDSP output *ya*[*n*]. Error detection is accomplished by comparing the difference *ya*[*n*] − *yr*[*n*]| against a threshold *Th*. Once the difference between *ya*[*n*] and *yr*[*n*] is larger than *Th*, the output *y*ˆ[*n*] is *yr*[*n*] instead of *ya*[*n*]. As a result, *y*ˆ[*n*] can be expressed as,

$$\hat{y}[n] = \begin{cases} y_a[n], & \text{if } |y_a[n] - y_r[n]| \le Th \\ y_r[n], & \text{if } |y_a[n] - y_r[n]| > Th. \end{cases}$$

Th is determined by

$$Th = \max_{\forall \text{input}} |y_o[n] - y_r[n]|$$

Where *yo*[*n*] is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation.

III. Proposed ANT Multiplier Design Using Fixed Width RPR

In this paper, we have a tendency to more planned the fixed-width RPR to interchange the full-width RPR block within the hymenopter style, as shown in Fig. 2, which might not solely give higher computation exactness, lower power consumption, and lower space overhead in RPR, however conjointly perform with higher SNR, a lot of space economical, lower operative offer voltage, and lower power consumption in realizing the hymenopter design. we have a tendency to demonstrate our fixed-width RPR-

based hymenopter style in Associate in Nursing hymenopter number.

The fixed-width styles ar sometimes applied in DSP applications to avoid infinite growth of bit breadth. Isolating n-bit least important bit (LSB) output may be a widespread answer to construct a fixed-width DSP with n-bit input and n-bit output. The hardware complexness and power consumption of a fixed-width DSP is typically concerning 1/2 the full-length one. However, truncation of LSB half ends up in rounding, that must be paid exactly. Several literatures are conferred to cut back the misreckoning with constant correction price or with variable correction price. The circuit complexness to compensate with constant corrected price may be less complicated than that of variable correction value; but, the variable correction approaches at sometimes a lot of precise.

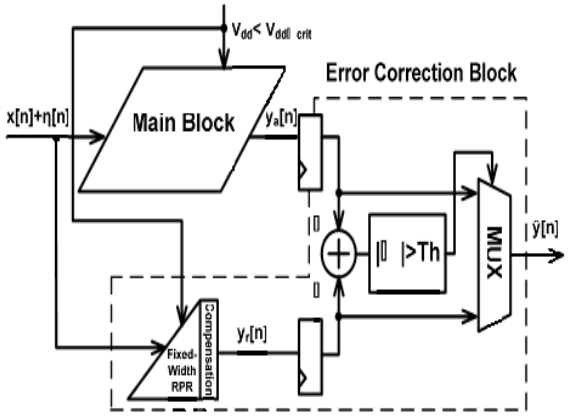

Fig.2. Proposed ANT architecture with fixed-width RPR.

In their compensation technique is to compensate the miscalculation between the full-length multiplier factor and also the fixed-width multiplier factor. However, within the fixed-width RPR of associate emmet multiplier factor, the compensation error we'd like to correct is that the overall miscalculation of MDSP block. Unlike, our compensation technique is to compensate the miscalculation between the full-length MDSP multiplier factor and also the fixed-width RPR multiplier factor. In today, there ar several fixed-width multiplier factor styles applied to the full-width multipliers. However, there's still no fixed-width RPR style applied to the emmet multiplier factor styles. to attain a lot of precise error compensation, we have a tendency to compensate the miscalculation with variable correction worth. we have a tendency to construct the error compensation circuit in the main exploitation the partial product terms with the biggest weight within the least important section. The error compensation formula makes use of chance, statistics, and regression analysis to search out the approximate compensation worth. to avoid wasting hardware quality, the compensation vector within the partial product terms with the biggest weight within the least important section is directly inject into the fixed-width RPR, that doesn't want further compensation logic gates. To any lower the compensation error, we have a tendency to conjointly think about the impact of truncated merchandise with the second most vital bits on the error compensation. We have a tendency to propose a slip-up compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, we locate the compensation circuit in the noncritical path of the fixed-width RPR. As compared with the full-width RPR design in, the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption.

A. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

In the hymenopter style, the perform of RPR is to correct the errors occurring within the output of MDSP and maintain the SNR of whole

system whereas lowering provide voltage. within the case of exploitation fixed-width RPR to comprehend hymenopter design, we tend to not solely lower circuit space and power consumption, however conjointly accelerate the computation speed as compared with the standard full-length RPR. However, we want to compensate immense misestimating attributable to pruning several hardware components within the LSB a part of MDSP. In the MDSP of *n*-bit ANT Baugh Wooley array multiplier, its two unsigned *n*-bit inputs of *X* and *Y* can be expressed as

$$X = \sum_{i=0}^{n-1} x_i \cdot 2^i, \qquad Y = \sum_{j=0}^{n-1} y_j \cdot 2^j.$$

The multiplication result *P* is the summation of partial products of *xi y j*, which is expressed as

$$P = \sum_{k=0}^{2n-1} p_k \cdot 2^k = \sum_{j=0}^{n-1} \sum_{i=0}^{n-1} x_i y_j \cdot 2^{i+j}.$$

The (*n*/2)-bit unsigned full-width Baugh–Wooley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(*β*)], minor ICV [MICV(*α*)], and LSP, as shown in Fig. 3. In the RPR, only MSP part is kept and the other parts are removed. Therefore, the other three parts of ICV(*β*), MICV(*α*), and LSP are called as truncated part. The truncated ICV(*β*) and MICV(*α*) are the most important parts because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm. To evaluate the accuracy of a fixed-width RPR, we can exploit the difference between the (*n*/2)-bit fixed-width RPR output and the 2*n*-bit full-length MDSP output, which is expressed as,

$$\varepsilon = P - P_t$$

Where *P* is the output of the complete multiplier in MDSP and *Pt* is the output of the fixed-width multiplier in RPR. *Pt* can be expressed as

$$\begin{aligned} P_t &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i \\ &\quad + f\left(x_{n-1}y_{\frac{n}{2}}, x_{n-2}y_{\frac{n}{2}+1}, x_{n-3}y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}}y_{\frac{n}{2}+2}\right) \\ &\quad + f\left(x_{n-2}y_{\frac{n}{2}}, x_{n-3}y_{\frac{n}{2}+1}, x_{n-4}y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}}y_{n-2}\right) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i + f(\mathrm{ICV}) + f(\mathrm{MICV}) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i + f(\mathrm{EC}) \end{aligned}$$

Where *f(*EC*)* is the error compensation function, *f(*ICV*)* is the error compensation function contributed by the input correction vector ICV(*β*), and *f(*MICV*)* is the error compensation function contributed by minor input correction vector MICV(*α*). The source of errors generated in the fixed-width RPR is dominated by the bit products of ICV since they have the largest weight. It is reported that a low-cost EC circuit can be designed easily if a simple relationship between *f(*EC*)* and *β* is found. It is noted that *β* is the summation of all partial products of ICV. By statistically analyzing the truncated difference between MDSP and fixed-width RPR with uniform input distribution.

B. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

To realize the fixed-width RPR, we construct one directly injecting ICV(*β*) to basically meet the statistic distribution and one minor compensation vector MICV(*α*) to amend the insufficient error compensation cases. The

compensation vector ICV(β) is realized by directly injecting the partial terms of $Xn-1$ $Yn/2$, $Xn-2Y(n/2)+1$, $Xn-3Y(n/2)+2$,. . ., $X(n/2)+2Yn-2$. These directly injecting compensation terms are labeled as $C1$, $C2$, $C3$,. . ., $C(n/2)-1$ in Fig. 3.The other compensation vector used to mend the insufficient error compensation case is constructed by one conditional controlled OR gate. One input of OR gate is injected by $X(n/2)Yn-1$, which is designed to realize the function of compensation vector β. The other input is conditional controlled by the judgment formula used to judge whether $\beta = 0$ and $\beta l = 0$ as well.

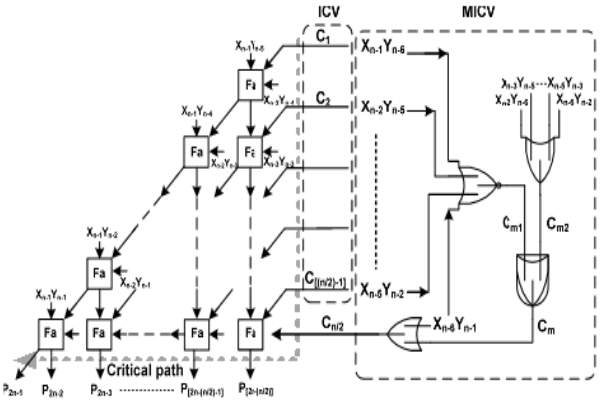

Fig. 3. Proposed high-accuracy fixed-width RPR multiplier with compensation constructed by the multiple truncation EC vectors combined ICV together with MICV

The term Cm1 is used to judge whether $\beta = 0$ or not. The judgment function is realized by one NOR gate, while its inputs are $Xn-1$ $Yn/2$, $Xn-2Y(n/2)+1$, $Xn-3Y(n/2)+2$,. . ., $X(n/2)+2Yn-2$. The term $Cm2$ is used to judge whether $\beta l = 0$. The judgment function is realized by one OR gate, while its inputs are $Xn-2Yn/2$, $Xn-3Y(n/2)+1$, $Xn-4Y(n/2)+2$,. . ., $X(n/2)+1$ $Yn-2$. If both of these two judgments are true, a compensation term Cm is generated via a two-input AND gate. Then, Cm is injected together with $X(n/2)Yn-1$ into a two-input OR gate to correct the insufficient error compensation. Accordingly, in the case of $\beta = 0$ and $\beta l = 0$ as well, one additional carry-in signal $C(n/2)$ is injected into the compensation vector to modify the compensation value as $\beta + 1$ instead of β. Moreover, the carry-in signal $C(n/2)$ is injected in the bottom of error compensation vector, which is the farthest location away from the critical path. Therefore, not only the error compensation precision in the fixed-width RPR can be enhanced, the computation delay will also not be postponed. Since the critical supply voltage is dominated by the critical delay time of the RPR circuit, preserving the critical path of RPR not be postponed is very important. Finally, the proposed high-precision fixed-width RPR multiplier circuit is shown in Fig. 3. In our presented fixed-width RPR design, the adder cells can be saved by half as compared with the conventional full-width RPR. Moreover, the proposed high-precision fixed-width RPR design can even provide higher precision as compared with the full-width RPR design.

IV. SIMULATION OF PROPOSED RPR

The written Verilog HDL Modules have successfully simulated and verified using Modelsim6.4b and synthesized using Xilinxise13.2.

Synthesis Results:

RTL schematic

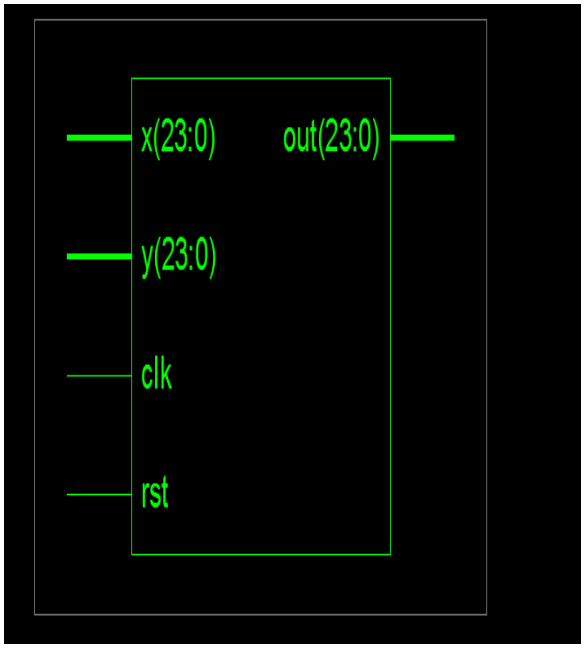

Fig.4.Proposed RPR block

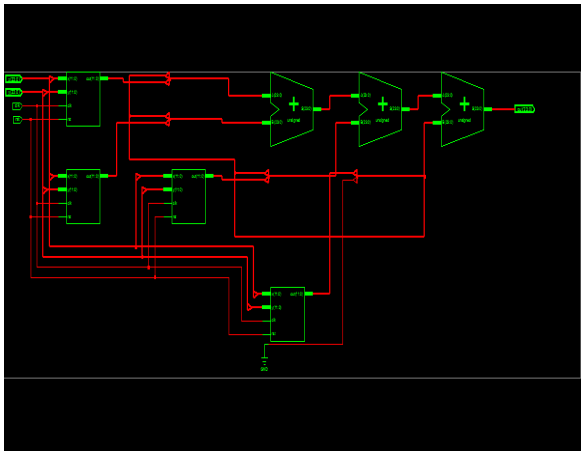

Fig.5.Schematic of the Proposed architecture

Timing Report:

```
Data Path: m5/out_0 to out<11>
                                   Gate     Net
  Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FDR:C->Q              2   0.514   0.532  m5/out_0 (m5/out_0)
   LUT2:I0->O            1   0.612   0.000  m3/Msub_w_lut<0> (m3/Msub_w_lut<0>)
   MUXCY:S->O            1   0.404   0.000  m3/Msub_w_cy<0> (m3/Msub_w_cy<0>)
   MUXCY:CI->O           1   0.052   0.000  m3/Msub_w_cy<1> (m3/Msub_w_cy<1>)
   MUXCY:CI->O           1   0.052   0.000  m3/Msub_w_cy<2> (m3/Msub_w_cy<2>)
   MUXCY:CI->O           1   0.051   0.000  m3/Msub_w_cy<3> (m3/Msub_w_cy<3>)
   MUXCY:CI->O           1   0.051   0.000  m3/Msub_w_cy<4> (m3/Msub_w_cy<4>)
   MUXCY:CI->O           1   0.051   0.000  m3/Msub_w_cy<5> (m3/Msub_w_cy<5>)
   MUXCY:CI->O           1   0.051   0.000  m3/Msub_w_cy<6> (m3/Msub_w_cy<6>)
   MUXCY:CI->O           1   0.051   0.000  m3/Msub_w_cy<7> (m3/Msub_w_cy<7>)
   MUXCY:CI->O           1   0.051   0.000  m3/Msub_w_cy<8> (m3/Msub_w_cy<8>)
   MUXCY:CI->O           1   0.051   0.000  m3/Msub_w_cy<9> (m3/Msub_w_cy<9>)
   XORCY:CI->O           1   0.699   0.509  m3/Msub_w_xor<10> (m3/w<10>)
   LUT2:I0->O            1   0.612   0.000  m3/Mcompar_s_cmp_le0000_lut<3> (m3/Mco
   MUXCY:S->O           12   0.752   0.969  m3/Mcompar_s_cmp_le0000_cy<3> (m3/s_cm
   LUT2:I0->O            1   0.612   0.357  m4/y<9>1 (out_9_OBUF)
   OBUF:I->O                 3.169          out_9_OBUF (out<9>)
  ----------------------------------------
  Total                     10.204ns (7.837ns logic, 2.367ns route)
                                     (76.8% logic, 23.2% route)

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Simulation Results:

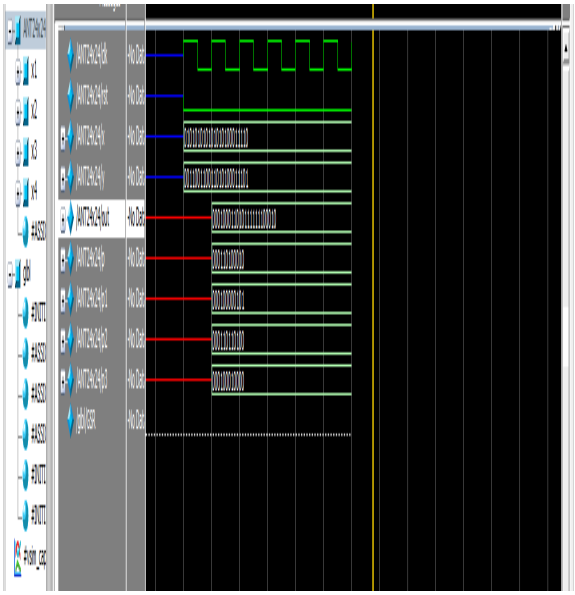

Fig.6.Simulation results

Extension

In this we propose a low error and area efficient fixed width RPR based 24*24 bit ANT multiplier. The low-voltage low-power merit in the presented ANT design can still be preserved under process deviation and high-temperature environments. In this we use four 12*12 ANT multipliers .As we are using 24*24 bit width we can efficiently use our project in real time applications.

V. CONCLUSION

In this paper, a low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. The proposed 12-bit ANT multiplier circuit is implemented in TSMC 90-nm process and its silicon area is 4616.5 μm2. Under 0.6 V supply voltage and 200-MHz operating frequency, the power consumption is 0.393 mW. In the presented 12-bit by 12-bit ANT multiplier, the circuitry area in our fixed-width RPR can be saved by 45%, the lowest reliable operating supply voltage in our ANT design can be lowered to 0.623 *V*DD, and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

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