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SEVEN LEVEL HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR INVERTER

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Abstract— Multilevel converters are the attractive solution for medium and high-power applications This paper proposes a new seven -level hybrid topology combining features of neutral point clamped and flying capacitor inverters.. This paper presents the seven level inverter with harmonics reduction. The harmonic reduction is achieved by selecting appropriate switching angles. The features of the proposed topology are investigated and compared to other available topologies. Simulation results are provided to verify the performance of the converter for medium voltage applications.

I.INTRODUCTION

Multilevel inverters are the important one which is mainly needed in the power industry .It may be easier to produce a high power and high voltage to control the voltage stresses in their structure. when the number of voltage levels in the inverter is increased, then considerably power ratings can also improved. Multilevel voltage source inverters allows them to reach high voltages by increasing the levels and decreasing the harmonics.

The main drawbacks in power electronic converter are switching loss, harmonics and voltage stress in the switches ,which are overcome by the advanced multilevel inverters. Although the multilevel inverters are initially introduced to reduce the harmonic content, it is found that the DC bus voltages could be increased beyond the voltage ratings of an individual power device by the use of voltage clamping network consisting of diodes[iv]. Multilevel inverters also improve the harmonic performance greatly without having to resort to PWM techniques. For medium voltage inverters, cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) are the primary topologies. Among them, ANPC and FC provide a common dc-link which is a strict requirement for many applications. FC inverter uses capacitors to generate output voltage levels. The availability of intra-phasal redundant states in this topology can provide both capacitor voltage balancing and power loss distribution among switches.

However, increased number of flying capacitors at higher levels that increases the initial cost and maintenance surcharges and decreases the reliability of the inverter along with the capacitor precharge in some applications are the main drawbacks of this topology. NPC inverter uses diodes to clamp the voltage levels generated at the dc-link capacitors to the output.

Excessive number of diodes, unbalanced operation of dc-link's voltage divider capacitors, and uneven distribution of loss among switches are major problems of this topology. Space vector algorithms are available to alleviate the unbalanced loss and capacitor voltage problems based on the inverter's operating condition. Active NPC (ANPC) improves the loss distribution of NPC by replacing diodes with active switches providing alternative neutral point path. The 7-level FC-ANPC is an example of hybrid topologies that made its way to the industry.

The ACS2000 family of medium voltage drives, commercialized by ABB, uses this topology with both active and passive front end configurations. The main advantage of this topology is the use of a single flying capacitor to generate the output seven levels. Compared to other topologies that provide a common dc-link, FC-ANPC has provided an acceptable tradeoff between the cost, performance, and reliability for 7-level applications. The disadvantages of FC-ANPC are high number of switches, series connection of high voltage switches, and poor loss distribution.

The classic multilevel inverter topologies have serious problems when the inverter is used to obtain five or more levels. An NPC converter of more than three voltage levels has problem in

balancing the bus capacitor voltages even for a back-to-back connection of capacitors. Many modulation techniques and controls have been proposed to solve these kind of issues but it has been proven that extra hardware components or special modulating signals are required to balance the DC bus capacitors' voltage. The FC converters are usually limited to four levels of voltage due to the large size of the FCs . Finally, the CHB need some isolation to transfer active power. In this paper active neutral point clamped converter can be discussed for new seven level

II. THE PROPOSED TOPOLOGY AND OPERATION

The circuit diagram for seven level FC based ANPC converter is shown in fig 1. The seven-level ANPC converter is the combination of two FC with a three-level ANPC converter at the output side. Two flying capacitor voltages are kept at Vdc and 2Vdc respectively to get the seven level output voltage. For simplification, last capacitor is maintained at Vdc . At the same time two DC link capacitor voltages are maintained at 3Vdc, the total voltage taken as 6Vdc. Switches Sc1, Sc2 and Sc3 has to withstand the voltage equal to Vdc, where the outer switch S1 need to withstand three times of this voltage due to voltage stress.

The seven level converter operates in two distinct half periods. During positive half period upper DC link capacitor(c1) is connected to a phase and during negative half period where the lower DC link capacitor (c2) is used to be connected. During these half-periods, the topology simplifies to a four-level FC converter [10] and for which the FC balancing requirements can be identified [14]. The equivalent circuits for one phase of the converter during the two half-periods of operation are given in Fig.3. To reduce the stress across the switches and to limit the losses in the outer switches, fundamental frequency is used as switching frequency.

This fundamental frequency operation on outer switch S1 limits the operating states of the three level ANPC from six modes to four modes and this is combination with the two states of the two flying capacitor cells, total switching states of the converter is sixteen for seven level FC based ANPC inverter.

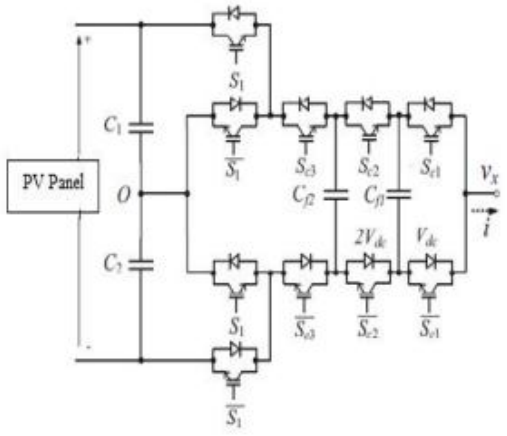
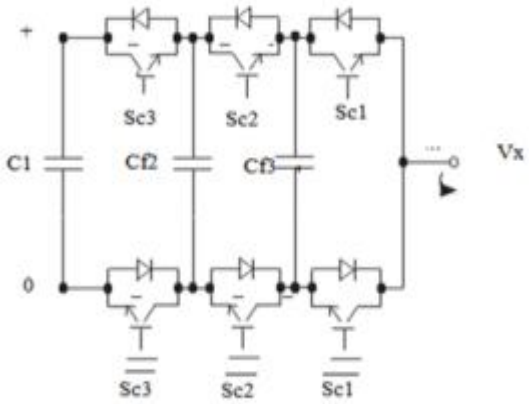
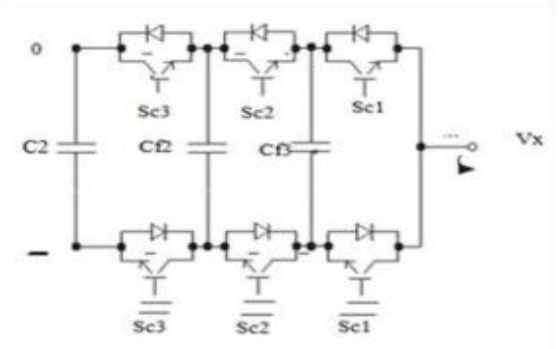


Fig. 1. A phase leg of the proposed 7-level hybrid topology



(a)



(b)

(a) Positive half period (b) negative half period

Fig 2: Equivalent circuit during Half period of operation

The switching states are given in the table. The voltage levels of ±2Vdc and ±Vdc can be designed with three different switching combinations and the required switching states to acquire these levels shows a way to balance the voltages across the neutral point and FCs voltage. Two states will provide the zero voltage state, due to its fundamental switching frequency at the outer

Flying Capacitors are based on selection of the proper switching state to maintain both FC to their individual reference values. It is important for the proper control operation of the converter .Selection of switching cells used in the converter will affect the FC voltage and the neutral point voltage (difference between the lower and upper DC link capacitor voltages VC1 - VC2). The proper voltage regulation of the converter can be observed using simulation circuits. The tabulation consists of various switching states to represent the voltage of different states of various voltage levels .the upper levels are represented using positive levels and the lower levels are represented by their negative voltages.

TABLE I.

SWITCHING STATES OF THE PROPOSED INVERTER

	S1	Sc3	Sc2	Sc1	OUTPUT VOLTAGE
V1	0	0	0	0	-3Vdc
V2	0	0	0	1	-2Vdc
V3	0	0	1	0	-2Vdc
V4	0	0	1	1	-2Vdc
V5	0	1	0	0	-Vdc
V6	0	1	0	1	-Vdc
V7	0	1	1	0	-Vdc
V8	0	1	1	1	(-)0
V9	1	0	0	0	(+)0
V10	1	0	0	1	+Vdc
V11	1	0	1	0	+Vdc
V12	1	0	1	1	+Vdc
V13	1	1	0	0	+2Vdc
V14	1	1	0	1	+2Vdc
V15	1	1	1	0	+2Vdc
V16	1	1	1	1	+3Vdc

III. MODULATION TECHNIQUES

Various modulation techniques may be adapted for the proposed topology. Carrier-based modulation with sinusoidal or modified reference as well as non-carrier-based techniques such as space vector modulation and selective harmonic elimination may be used to generate the gate signals. The choice of a modulation technique is mostly a tradeoff among the requirements of the application, complexity of the software, and cost of the control hardware

A. Carrier-Based Modulation

Carrier set's arrangement and reference waveform's shape are the main sources of varieties in carrier-based modulation techniques for multilevel inverters.

As for carrier set's arrangement, level shifted carriers LSC and phase shifted carriers PSC are the two main categories that are respectively suitable for diode-clamped and multi-cell structures.

Two members in the LSC family, alternative phase opposition disposition APOD and phase disposition PD areknown to generate the best results for singe-phase and threephase applications, respectively. PSC in its original form has been shown to generate a PWM waveform that matches with APOD. Also a modified version of PSC with dynamic phase shift has been shown to match with PD . The reference for single-phase applications is usually a simple sinusoidal waveform.

For three-phase applications, a variety of reference waveforms are available due to the possibility of common mode injection in three-phase structure. This flexibility has been used to serve different purposes such as increased dc link utilization, lower THD, lower Loss, and neutral point voltage control. For the proposed inverter, a hybrid modulation technique is required due to the hybrid structure of the topology.

For three-phase case, similar approach may be adopted except that, to generate a PD scheme equivalent, the positive cycle carriers should have $\pi/2$ phase shift compared to the negative cycle carriers. Also, the carriers incorporate a dynamic phase shift which for sampled reference waveforms always adds up by $\pi/2$ at the carrier band transitions. For the reference waveform, centered space vector PWM

(CSVPWM) sampled at half PD carrier period can provide similar output performance as SVM. Figure 4 illustrates the modulation technique using sampled CSVPWM along with modified PSC for the proposed inverter.

B. Non-Carrier-Based Modulation

For non-carrier-based modulation techniques such as SVM and SHE, the output PWM waveform may be generated first and then decomposed to the required switching signals. It is important to note that this procedure is independent of the adopted modulation technique. Therefore, it can be used with carrier-based modulation techniques as well as non carrier-based. This might be a good alternative when the complexity of the carrier-based technique is relatively high e.g. for PD scheme.

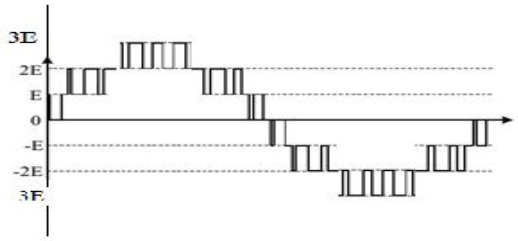


Fig.3 . Output waveforms of both Carrier-based modulation using modified PSC with sampled CSVPWM reference for three phase application and Output waveform of Carrier-based modulation using PSC with sinusoidal reference for single phase application.

IV. COMPARISON WITH OTHER TOPOLOGIES

The 7-level ANPC has low switch count but the major problems are unbalanced operation of dc-link capacitors, poor loss distribution among switches, and excessive number of diodes. 7-Level FC provides low switch count and excellent loss distribution but requires high number of flying capacitors that can adversely affect the initial cost, maintenance and replacement surcharges, and reliability of the inverter. Capacitors' precharge requirement in some applications is also a drawback of this topology.

The 7-level SMC topology provides lower capacitor count compared to FC and good loss distribution. However, high switch count and high frequency switches in series are the main issues of this topology. The 7-Level FC ANPC provides a good balance between the number of semiconductors and capacitors. The major issue with this topology is the poor loss distribution among the switches. The topology proposed in this paper, provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connection of semiconductor devices, keep the balanced operation of dclink capacitors while keeping the number of costly components such as capacitors and switches as small as possible.

V. SIMULATION RESULTS

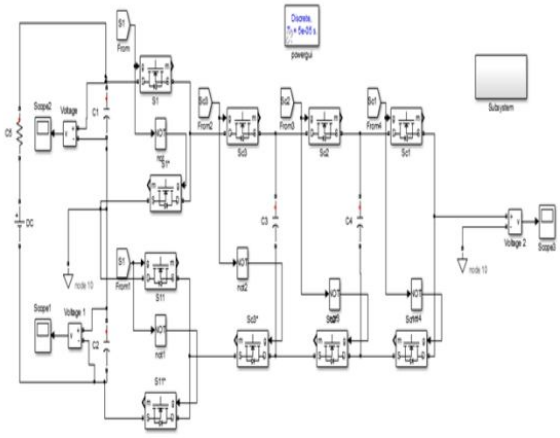
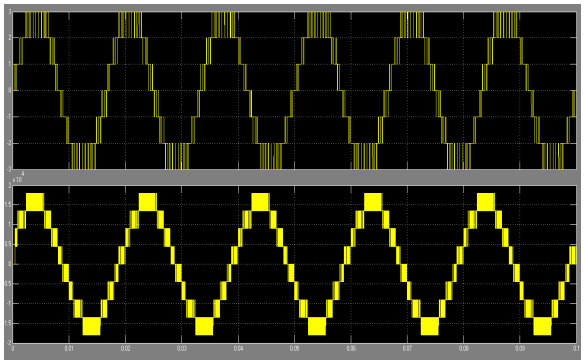
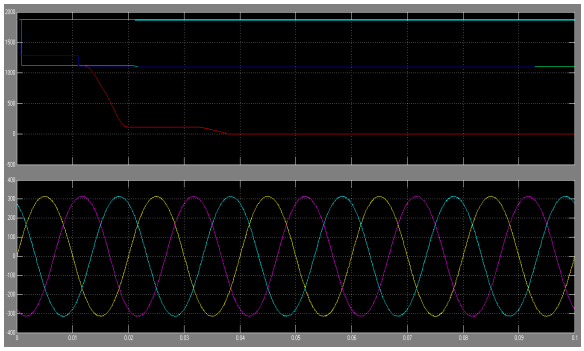


Fig.4 7L-ANPC simulation diagram

To verify the operation of the proposed topology and the performance of the modulation techniques provided, a model is developed and simulated with PSIM software. Centered space vector modulation (CSVPWM) is used at modulation index of 1.09 and carrier frequency 5kHz.



(a)



(b)

Fig. 5. Simulation results. (a) Phase voltage and Line voltage (b) Flying capacitor voltages, Load current

VI. CONCLUSION

A new hybrid 7-level inverter topology and modulation technique is proposed. The harmonics are reduced due to increasing of the multi levels However, since the capacitors still see the switching frequency and their size remain the same, it is expected to reduce the inverter's total cost. Also, unlike 7-level ANPC, all switches must withstand the same voltage which eliminates the need for series connection of switches and associated simultaneous turn on and off problem. Good loss distribution among switches can increase the inverters rated power or provide higher switching frequency and smaller capacitor size.

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