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Performance Analysis and Development of an Efficient Double Tail Comparator for A/D Convertors

J. B. KISHORE KUMAR
[1]jbkishorekumar@gmail.com
[1]PG Scholar, Dept of ECE, Sreenivasa Institute of Technology and Management(Autonomous), Murkambattu, Chittoor, JNTU Anantapur University,

ABSTRACT:

The need for an ultra low-power, area efficient, and high speed Analog-to-Digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this project, an analysis on the speed and power factors of the available dynamic comparators presented and are analysed. From the analytical expressions, designers can obtain an instinctive knowing about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, an efficient new dynamic comparator is explored, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced power. Simulation with respect to different CMOS technology that confirm the analysis results. It is shown that in dynamic comparator both the power consumption and delay time is significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 GHz and 1.1 GHz at supply voltages of 1.2 and 0.7 V, while consuming 8.4 μW and 4.11 μW respectively.

Index Terms—Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs),low-power analog design.

I. INTRODUCTION

Comparator circuits are widely used to compare physical measurements, which are provided and those physical variables to be translated into voltage signals. Comparator is one of the basic building blocks in most of the analog-to-digital converters (ADCs).Many high- speed ADCs, such as flash ADCs, high-speed, low power comparators with small die area.

High-speed comparators in ultra deep sub-micrometer(UDSM) the CMOS technologies suffer with low supply voltages especially when considering the fact that threshold voltages of the devices which is not scaled at the same pace as supply voltages of the modern CMOS processes[1]. Hence, designing the high-speed comparators is more challenging when supply voltage is smaller.

In other words, the technology, to achieve a high speed, larger transistors are required to compensate reduction of supply voltage, which means more die area and power is needed. Apart that, low-voltage operation results in limited common-mode input range, which is important in many of high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods[2][3], current-mode design and those using dual-oxide processes, which use higher supply voltages are developed to meet the low-voltage design challenges.

Apart from technological modifications, developing a new circuit structures which avoid stacking many transistors in between the supply rails is preferable for low-voltage operation[4], especially if they do not maximize the circuit complexity. In additional circuit is added to conventional dynamic comparator to enrich the comparator speed in low supply voltages.

When there is a need for comparator circuit, it is always best to use for a comparator chip as the basis of the circuit. Comparator chips are better at handling switching between any two values and may often output stages that can more easily interface with the logic than of analogue operational amplifiers. By means of the basic circuit operation, the main difference is most comparators that have open collector output and require an external pull-up resistor. As they employ this form of output. It is very easy to interface with logic circuitry.

In electronics, Operational amplifier which is designed to be used with a negative feedback. It can be used as comparator in the open loop configuration. On the other hand, Comparator is mainly designed for open loop configuration without any feedback. so, it is the most widely used device in the electronic circuits. Comparators which are mostly used in analog-to-digital converter (ADCs). In this process, first input signal is sampled. Then the sampled signals which those are applied to a number of comparators to determine the digital equivalent of the analog value. Also, comparators are used in peak detectors, BLDC operating motors, switching power regulators.

II. Principal of Conventional Dynamic Comparator

The conventional dynamic comparator schematic diagram which is most widely used in A/D converters, with a high input impedance, rail-to-rail output swing, and also no static power consumption is shown in Fig.

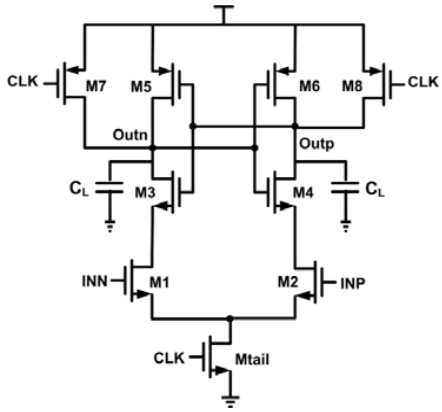

Figure 1. Schematic diagram of the conventional dynamic comparator.

The operation of the comparator is shown below:

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1.The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa

and the delay of this comparator is comprised of two time delays, t0 and tlatch. The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e., VINP > VINN), the drain current of transistor M2 (I2) causes faster discharge of Outp node compared to the Outn node, which is driven by M1 with smaller current. Consequently, the discharge delay (t0) is given by

$$t_o = \frac{C_L|V_{thp}|}{I_2}$$

$$to \cong 2\frac{C_L|V_{thp}|}{I_{tail}} \quad \text{------(1.1)}$$

since in equation (1.1)

$$I_2 = \frac{I_{tail}}{2} + \Delta I_{in} = \frac{I_{tail}}{2} + g_{m1,2}\,\Delta V_{in}$$

for small differential input (Vin), I2 can be approximated to be constant and equal to the half of the tail current. The second term, tlatch, is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of Vout = VDD/2 has to be obtained from an initial output voltage difference V0 at the falling output (e.g., Outp). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch. Hence, the latch delay time is given by

$$t_{latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_o}\right) \quad \text{------}$$

(1.2)

Where gm, eff is the effective transconductance of the back-to-back inverters. In fact, this delay depends, in algorithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at t = t0). Based on (1), ΔV0 can be calculated from

$$\Delta V_o = \left|V_{outp}(t = to) - V_{outn}(t = to)\right|$$

$$\Delta V_o = \left|V_{thp}\right| - \frac{I_2 t_o}{C_L}$$

$$\Delta V_o = \left|V_{thp}\right|\left(1 - \frac{I_2}{I_1}\right) \quad \text{-(1.3)}$$

The current difference, ΔIin = |I1 − I2|, between the branches is much smaller than I1 and I2. Thus, I1 can be approximated by Itail/2 and (3) can be rewritten as

$$\Delta V_o = \left|V_{thp}\right|\frac{\Delta I_{in}}{I_1}$$

$$\Delta V_o \approx 2\left|V_{thp}\right|\frac{\Delta I_{in}}{I_{tail}}$$

$$\Delta V_o \cong 2\left|V_{thp}\right|\frac{\sqrt{\beta_{1,2} I_{tail}}}{I_{tail}}\Delta V_{in}$$

$$\Delta V_o = 2\left|V_{thp}\right|\sqrt{\frac{\beta_{1,2}}{I_{tail}}}\Delta V_{in} \quad \text{-}$$

(1.4)

In this equation, β1,2 is the input transistors current factor and Itail is a function of input common-mode voltage (Vcm) and VDD. Now, substituting V0 in latch delay expression and considering t0, the expression for the delay of the conventional dynamic comparator is obtained as

$$t_{delay} = t_o + t_{latch}$$

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} X \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \text{-}$$

(1.5)

Above equation explains the impact of various parameters. The total delay is directly proportional to the comparator load capacitance CL and inversely proportional to the input difference voltage (Vin). Besides, the delay depends indirectly to the input common-mode voltage (Vcm). By reducing Vcm, the delay t0 of the first sensing phase increases because lower Vcm causes smaller bias current(Itail). On the other hand, (4) shows that a delayed discharge with smaller Itail results in an increased initial voltage difference V0), reducing tlatch. Simulation results show that the effect of reducing the Vcm on increasing oft0 and reducing of tlatch will finally lead to an increase in the total delay. In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistorsM3 and M4, where the gate source voltage of M5 and M6is also small; thus, the delay time of the latch becomes large due to lower trans-conductances. Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favourable for regeneration.

III.CLOCKED REGENERATIVE COMPARATORS

A.DOUBLE TAIL DYNAMIC COMPARATOR

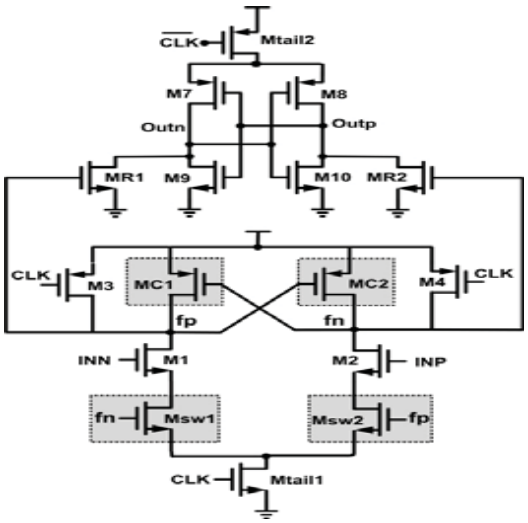

Figure 2.double tail dynamic comparator

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure.

The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3 /M4 transistors but in a cross-coupled manner.

The operation of the proposed comparator is as follows. When clk = 0, the reset phase, both the tail transistors Mtail1 and Mtail2 are in off to avoiding static power. Transistor M3 and M4 are in on. M3 and M4 pulls both fn and fp nodes to Vdd, hence transistor MC1 and MC2 are cut off. The circuit has two intermediate stage transistors MR1 and MR2. These transistors reset both latch outputs to ground. During decision-making phase, clk = Vdd, both the tail transistors are on, M3 and M4 transistors are off. At the beginning of this phase, the control transistors MC1 and Mc2 are still off (since fn and fp are about Vdd). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (MC1 in this case) starts to turn on, pulling fp node back to the Vdd, so another control transistor remains off, allowing fn to be discharged completely.

Fig.2 represents the output waveform of double tail comparator. When one of the control transistors turns on, a current from Vdd is drawn to the ground via input and tail transistor (ie, MC1, M1, and Mtail1) result in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors such asMsw1 and Msw2. As soon as the comparator detects that one of the fn or fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the Vdd and fn should be discharged completely, hence the switch in the charging path of fp will be opened, but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

B.DOUBLE TAIL COMPARATOR USING SWIT-CHING TRANSISTORS

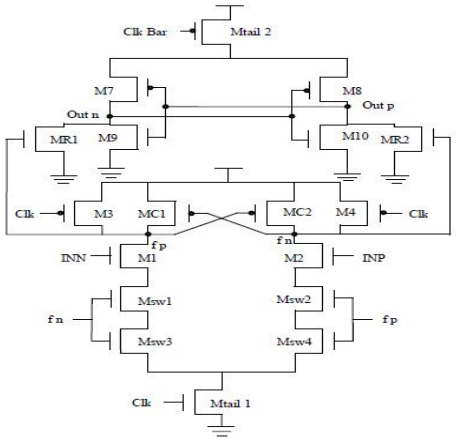

Fig 3.double tail comparator using switching transistors.

Compared with proposed it provides, better performance of double tail comparator in low voltage applications. Drawback of proposed comparator is ,the nodes fn and fp starts to drop with different rates according to the input voltages. The continues falling of fn, the corresponding transistor MC1 starts to turn on and fp node backs to VDD. Node fn to be discharged completely(MC2 off).When one of the control transistors (MC1) turns ON, a current from VDD is drawn to the ground via input and tail transistor. Resulting a static power consumption. For this purpose two switching transistors (Msw3 and Msw4) have been added to Msw1 and Msw2 in series manner.

Modified comparator reduced the delay and power. Fig shows the schematic diagram of the double tail comparator using switching transistors. Due to the better performance of double tail architecture in low voltage applications the comparator is designed based on the double-tail structure. The main idea of the proposed comparator is

to increase ΔVfn/fp in order to increase the latch regeneration speed. Two more transistor connected below the Msw1 and Msw2 , which is used for switching.

C.MODIFIED DYNAMIC DOUBLE COMPARATOR

As the proposed double tail comparator architecture shows better performance in low voltage applications, the modified comparator is designed based on the double tail structure. The main idea of the modified is to reduce the static power consumption by completely cut off the flow of leakage current to the ground. For this purpose two more transistors have been added.

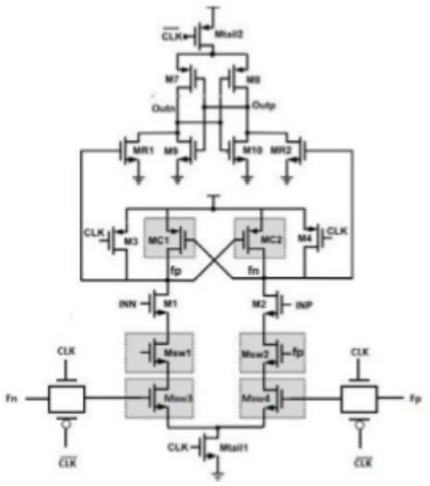

Fig.4 modified dynamic double comparator

Hence all the above existing comparator are analyzed with different cmos technology to get an efficient design that to be used in many electronic devices.

IV. DEVELOPMENT AND PERFORMANCE ANALYSIS

As the proposed double tail comparator architecture shows better performance in low voltage applications compared with all the existing models, the modified comparator is designed based on the double tail structure. The main idea of the modified is to reduce the static power consumption by completely cut off the flow of leakage current to the ground.

This model gets efficient results while differentiated with the existing model at different technologies. Hence, concluding that this structure gives better than others.

MODIFIED DOUBLE EDGE TRIGGERED STRUCTURE

In the proposed comparator circuit complexity is reduced. Number of transistors is reduced from 22 to 12. The new comparator is double edge triggered. It works for both the positive and negative edges of clock. Working principle of the proposed comparator is same as that of low voltage low power comparator. When clock is high M1 and M7 are off and M6 and M8 are on. When clock is low M6 and M8 are off and M1 and M7 are on. An input dependent differential voltage ΔVfn(p) will build up depending on change in input values. The intermediate stage formed by MR1 and MR2 passes ΔVfn(p) to the cross coupled inverters and also provides a good shielding between input and output. Depending on the difference in inputs we will get the output.

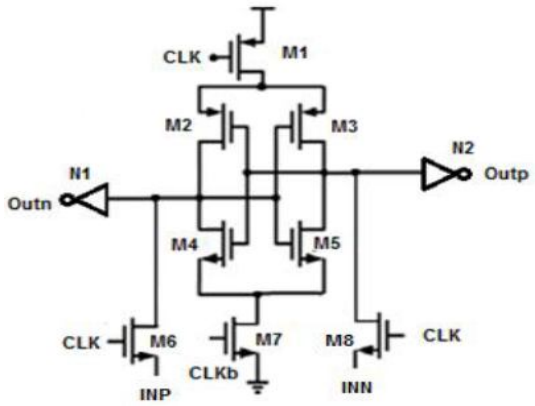

Fig.5 Schematic of double edge triggered structure.

PERFORMANCE ANALYSIS BY USING MICROWIND TOOL

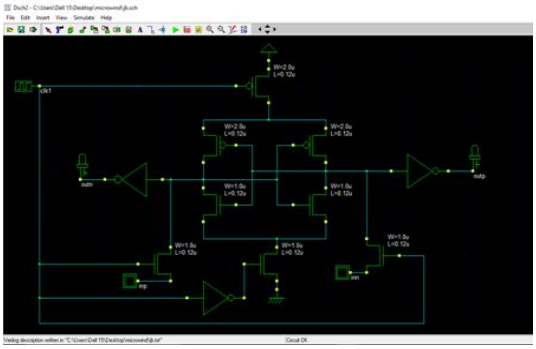

Fig.6 schematic of modified double edge triggered structure.

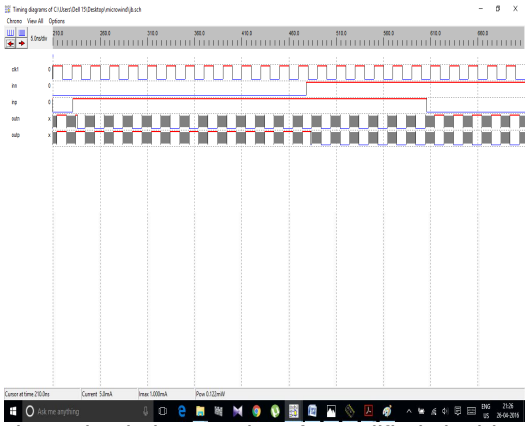

Fig.7 Simulation results of modified double edge triggered structure

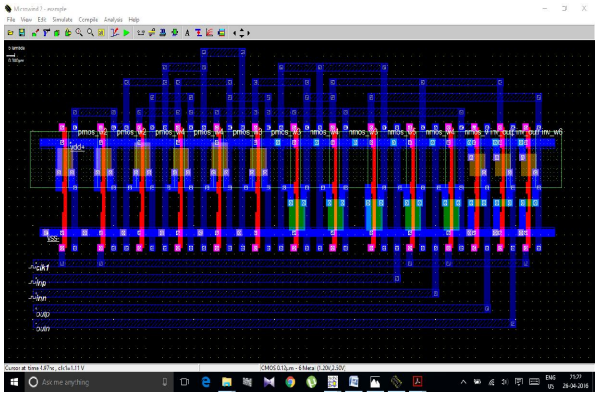

Fig.8 Layout of modified double edge triggered structure

V. COMPARATIVE ANALYSIS

In order to compare all the existing comparator with the conventional, double-tail dynamic comparators and modified double edge triggered comparator all circuits have been simulated in different 0.12-µm, 0.9-µm and 0.7-µm CMOS technology with VDD = 1.2V, 1.0V and 0.7V respectively. Comparators were optimized and transistor dimensions were scaled to an equal offset standard variation of σ OS = 8 mV at the input common- mode voltage of V cm =1.1V.

Type of Comparator / Parameter considered	Conventional Single-tail	Conventional Double-tail	Modified Double-tail	Further modified Double-tail	Double-tail using switching transistor	Modified -dynamic double	Dou edg trig
No of transistors used	9	14	16	18	20	24	
120nm cmos technology with 1.2V input voltage							
Power	2.770 µW	0.694mW	0.839mW	0.430mW	0.594mW	0.419mW	8.4
Area	21*12µm	27*15µm	32*9 µm	35*10 µm	38*10 µm	49*10 µm	20
90nm cmos technology with 1.0V input voltage							
Power	2.152 µW	0.497 mW	0.595 mW	0.308 mW	0.420 mW	0.314mW	6.1
Area	22*10 µm	28*12 µm	35*8 µm	38*9 µm	41*10 µm	51*13µm	51*
70nm cmos technology with 0.7V input voltage							
Power	1.273 µW	0.274 mW	0.331 mW	0.165 mW	0.221mW	0.157 mW	4.1
Area	16*8 µm	21*11 µm	26*8 µm	28*8 µm	30*8 µm	39*9 µm	16

table I :comparative analysis.

VI. CONCLUSION

Among the comparators studied the double-tail edge triggered comparator which has a back to back latch stage has the lowest power dissipation. Dynamic comparators have less dynamic power dissipation and input offset voltage compared to the pre-amplifier based comparator. But their speed is the latter due to the parasitic capacitances. The layout for the different comparators are given. Compared analysed the results of different types of comparator in different cmos technology are as shown in above table.

VII. FUTURE SCOPE

Offset voltage optimization and optimization of the circuits after layout can be one topic. Finding application specific comparators can be another topic. Further technology optimization can be another topic.

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