

# A Novel Level Shifter By Using A Modified Wilson Current Mirror

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**Abstract** - Wide-range level shifters play critical roles in ultra-low-voltage circuits and systems. Although state-of-the-art level shifters can convert a sub threshold voltage to the standard supply voltage, they may have limited operating ranges, which restrict the flexibility of dynamic voltage scaling. Therefore, this paper presents a novel level shifter, of which the operating range is from a deep sub threshold voltage to the standard supply voltage and includes upward and downward level conversion. The proposed level shifter is a hybrid structure comprising a modified Wilson current mirror and generic CMOS logic gates. The simulation and measurement results were verified using a 65-nm technology. The minimal operating voltage of the proposed level shifter was less than 200 mV based on the measurement results. In addition to the operating range, the delay, power consumption, and duty cycle of the proposed level shifter were designed for practical applications.

## I INTRODUCTION

Dynamic voltage scaling (dvs) has been widely used in digital processing elements for reducing energy consumption, and aggressive voltage scaling has extended the voltage range into the sub threshold region. The ultra-low power consumption of sub threshold operations facilitates the development of crucial applications, such as

ubiquitous sensors and miniature health-care devices. Near-threshold operations of processors and memories achieve the optimal energy consumption, whereas sub threshold operations further reduce power consumption, enabling the operations of autonomous sensor nodes that rely on energy scavenging. However, from a system perspective, sub threshold operations are limited to part of the digital processing elements. Other system components, such as the power management unit, radio, actuators, and sensors, have distinct constraints in the supply voltage, where sub-to-suprathreshold level conversion is usually unavoidable. General-purpose applications also require wide-range level shifters (LSs) if a system involves at least one aggressive DVS domain.

Wide-range LSs receive ultra- low voltage signals and use the weak drive current of pull-down networks (PDNs) to overcome the leakage of weakly conducting pull-up networks (PUNs). When input level is sub threshold, the conversion results of LSs are vulnerable and easily affected by process, voltage, and temperature variations. Therefore, several sub threshold LSs were proposed to solve this problem. Although these LSs can convert a sub threshold voltage, critical problems occur when using them in general DVS applications. First, previous sub threshold LSs may exhibit

timing issues when the input and output levels are close. Ultra-low-voltage (ULV) processors and memories usually support sub threshold and suprathreshold operations for enabling energy and performance trade-offs. Both wide-range and close -range level conversion are required to achieve this flexibility. When input and output levels are close, previous sub threshold LSs may have considerable skews in rising and falling delays because the drive strength of the PUNs was reduced. Although weak pull-up strength is favorable when input level is low, the rising delay increases considerably when the input level becomes high. Therefore, the operating range is confined.

In addition to the operating range, bidirectional LSs are critical for DVS applications. The voltage difference between two DVS domains can be either positive or negative; in other words, a cross-domain path may require upward and downward level conversion. Although a riskless solution may involve using a constant-voltage interface (such as a share bus), supplied with the highest voltage of the DVS range, this riskless architecture consumes extra power on the interface. Therefore, LSs with bidirectional level conversion improve the energy efficiency of the interface; however, this is a challenge for sub threshold LSs.

This paper presents novel LS that use a modified Wilson current mirror hybrid buffer (MWCMMHB). The proposed MWCMMHB LS was designed for full-range and bidirectional level conversion. The term “full range” indicates that the minimal

operating voltage can be deep sub threshold, close to the minimal supply voltage of digital circuits, and the maximal operating voltage is the standard supply voltage defined in a transistor technology. In addition to the operating range, the delay, power consumption, and duty cycle of LSs were carefully considered. The energy efficiency of wide-range level conversion was examined. The low slew rate of sub threshold signals may lead to a long transition period and consume high short-circuit power. To reduce this power consumption, robust sub threshold LSs require amendments with proper voltage assignment.

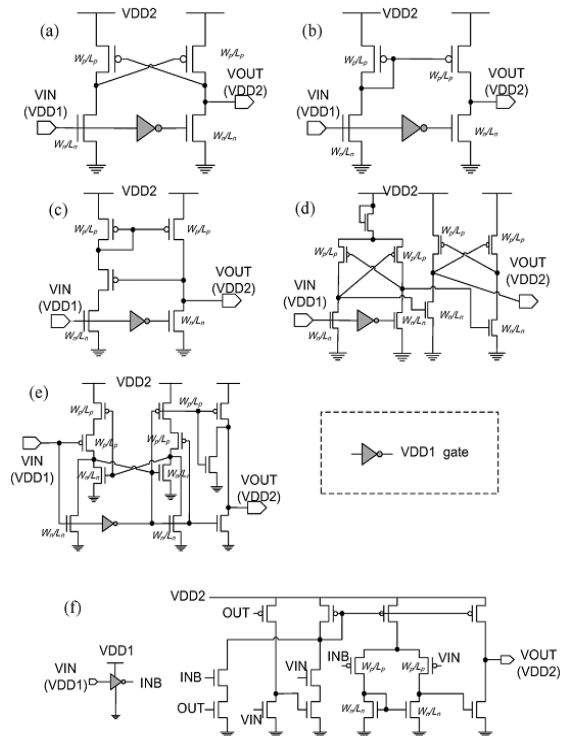


Fig.1. Conventional and related level shifters using. (a) a cross-coupled(CC) structure; (b) a current mirror(CM);(c) a Wilson current mirror(WCM); (d) a two-stage cross-

coupled structure (TSCC); (e) cross-coupled NOR gates and part of a NOR gate (CCPNR); (f) a logic error correction circuit (LECC). The transistors labeled  $W_T$  were set equal for fair structural comparisons in Section III.B.

## II SUBTHRESHOLD LEVEL SHIFTER: SURVEYS AND QUALITATIVE COMPARISONS

Sub threshold LSs are surveyed in this section. A conventional cross-coupled (CC) LS is a differential cascade voltage switch logic (DCVSL) for raising a low voltage level, as shown in Fig. 1(a). The drive strength of NMOS transistors is enhanced to overcome the leakage of weakly conducting PMOS transistors. The operating range of CC LSs depends on the transistor threshold voltage ( $V_t$ ) and size; however, the operating range of CC LSs is difficult to extend to the sub threshold region (with respect to the NMOS  $V_t$ ) because the (WCM), which clamps the quiescent power consumption under a suprathreshold input. Fig. 1(d) shows a two-stage CC LS (TSCC), of which the pull-up driving strength is reduced by a header NMOS, which expands the convertible input voltage. Fig. 1(e) shows a CC-type LS (CCPNR), in which the output stage is a part of the NOR gate fed by the primary input to accelerate the overall LS speed. Fig. 1(f) is a CM-type LS that uses a logic error correction circuit (LECC), which monitors input and output signals to create an implicit pulse; the output updates data during the pulse.

Five qualities involved in using LS in wide-range DVS applications. The proposed LS satisfy all five qualities. Each quality and the comparison are described in the following paragraphs, and comparisons of the quantitative delay, power consumption, and duty cycle are presented in Section III.

### 1) Small area for sub threshold level conversion

A conventional CC LS requires an exponential increase in transistor size to convert a sub threshold level, whereas the area of a standard cell must be constrained. This quality was considered in recent works, and the sub threshold LSs referred to satisfy this basic criterion.

### 2) Low power consumption in Suprathreshold operations

High quiescent power consumption occurs in conventional CM and LECC LSs when they receive a suprathreshold voltage input. A CM LS has a high quiescent current because of the bias currents. Conversely, an LECC LS may have an excessively narrow LECC pulse to update the output, where the function fails, and a short-circuit path draws a high quiescent current.

### 3) Balanced rising and falling delay in the operating range

Balanced rising and falling delay ensures a 50% signal duty cycle. This criterion can be relaxed considering a long data path or a low clock frequency. However, the duty cycle of the WCM LS is problematic when its input

and output levels are close. Because of a weak PUN, the WCM LS has a long rising delay, which is up to one hundred times longer than the falling delay (Fig. 5). This severe signal skew is not easily tolerated.

#### 4) Size- & $V_t$ -insensitivity to the operating range

Transistor size and  $V_t$  may determine the operating range of LSs. Therefore, insensitivity to transistor size and  $V_t$  enables an LS to be applied to various technologies and to tolerate process variations. Analytically, CM types are superior to CC types in achieving this objective; the analyses have been presented in an earlier study. For CC-type LSs, the effective operating region usually depends on the transistor  $V_t$ . For example, the TSCC LS is a dual- $V_t$  design, but some sub threshold LSs may use triple- $V_t$  transistors, and other LSs use thick oxide and zero- $V_t$  transistors. In addition, LSs implemented using SOI may use body ties. However, because this work focused on LS structure and used single- $V_t$  transistors, only the TSCC LS was involved and adapted to a single-  $V_t$  version for comparison. Additional details are provided in the quantitative comparisons.

#### 5) Bidirectional level conversion

Conventionally, bidirectional LSs are optional for power-management expansion. Downward level conversion can be realized using only an inverter, unless the signal skew is highly sensitive. A conventional CC LS also sup-ports bidirectional level

conversion in the suprathreshold region. However, full-range bidirectional level conversion is challenging. Pull-up and pull-down strength must be analyzed for all combinations of input and output levels. CC, TSCC, and CCPNR LSs have limited bidirectional regions because of unbalanced pull-up and pull-down strength. The WCM and LECC LSs are suggested only for upward level conversion. Details of bidirectional level conversion are provided in Section III.B.

### III. PROPOSED LEVEL SHIFTING STRUCTURE AND QUANTITATIVE COMPARISONS

#### A. Proposed Level Shifting Structure

The proposed MWCMHB LS is a hybrid structure comprising a modified Wilson current mirror and CMOS logic gates. The input and output levels range from a sub threshold voltage to the standard supply voltage defined in a transistor technology. Bidirectional level conversion is available; that is, input and output levels can be scaled independently.

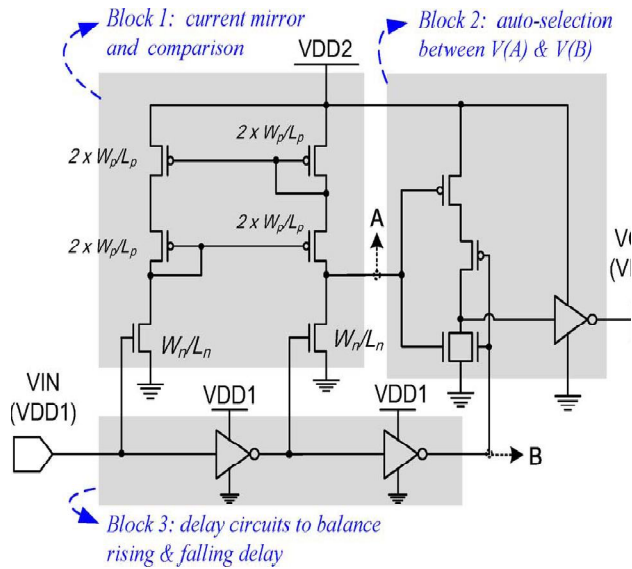


Fig.2. Proposed MWCMHB level shifter.

The proposed LS structure is illustrated with three circuit blocks, as shown in Fig. 2. A modified Wilson current mirror (MWCM) is located in Block 1. When VDD1 is sub threshold and VDD2 is high, the MWCM structure balances the rising and falling delay at Node A, without losing the original static bias that is favored in the WCM LS. However, when the VDD1 and VDD2 levels are close, the MWCM encounters the same problem as the WCM does: the cascade PMOS has insufficient drive currents and increases the rising delay. Therefore, in Block 3, a delay path is designed adaptively to reduce the rising delay and maintain a moderate duty cycle. An output inverter offers sufficient drive strength, which is required in a standard cell design. Unlike the CCPNR LS, which has a similar structure, the proposed LS uses a CM-type amplifier, a balancing delay path, and a complementary OR gate in Block 2. The CM-type structure provides a wide operating range, and the stacked PMOS

transistors in the complementary OR gate limit the leakage current.

## B. Characteristics and Comparisons

This section presents comparisons of the delay, power, and duty cycle of the proposed and reference LSs. The proposed and reference LSs were simulated using a 65-nm technology. For a fair comparison of circuit structure, the key transistors used the same  $V_t$ , width, and length.

The proposed MWCMHB, CC, WCM, and CCPNR LSs have similar static power consumption in the operating region. The CC and CCPNR LSs have high power consumption around the boundary of the failure region. The conventional CM LS is known for the high quiescent current at a suprathreshold voltage. The LECC LS fails when VIN is high and thus consumes high static power. The dashed lines indicate the failure region, where the power consumption is shown in case of any incorrect DVS operation.

A combined structure consisting of different LSs that are complementary in the operating region (e.g., CC-WCM combined LS). However, the overall power consumption must be considered if an LS fails in some operating ranges. For example, if CC and WCM LSs are combined, then high power consumption will occur around the failure boundary of the CC LS. To prevent high power consumption in this case, automatic multiplexing and power-gating control can be used; however, a high overhead in circuit design and system control is the drawback.

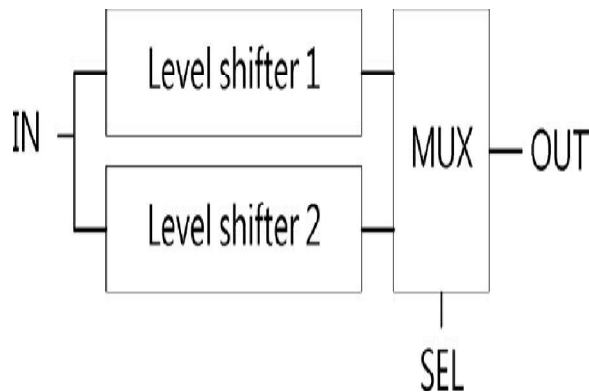


Fig.3. An available full-range level shifter structure; overheads in power consumption and automatic selection (SEL) must be considered

#### IV. ENERGY EFFICIENCY OF WIDE-RANGE LEVEL CONVERSION

The energy efficiency of wide-range level conversion requires a specific consideration of short-circuit power. A low-voltage input signal has a slow slew rate, which increases the transition time and short-circuit power of the high-voltage part of an LS. For the LSs that can convert sub-threshold signals (MWCMHB, CM, WCM, LECC), the row of  $V_{DD1}=0.1$  V and the column of  $V_{DD2}=1.2$  V in the power gradient is steep. This power consumption on the interface deteriorates the energy efficiency of a deep sub-threshold core. To solve this problem, robust sub-threshold LS may be adapted and cascaded into two stages. For clarity, simplified equations of the energy consumption of an ULV core and its interface are presented. The simulation results rather than analytical results are discussed here for application purposes.

## VI. CONCLUSION

A novel full-range level shifter was proposed for aggressive DVS applications. The delay, power consumption, and duty cycle of the proposed level shifter were verified for the full-range operability. The short-circuit power of converting deep sub-threshold signals was noted and can be solved by inserting a near-threshold supply voltage. Various simulations and measurements validated the proposed design. The minimal convertible voltage was less than 300 mV from the statistical simulations and less than 200 mV according to the measurement results.

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