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AN OPTIMIZED IMPLEMENTATION OF VEDIC MATHEMATICS MULTIPLIER USING VERILOG

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ABSTRACT:

The main purpose of the project is to improve the speed of the digital circuits like multiplier since adder and multiplier are one of the key hardware components in high performance systems such as microprocessors, digital signal processors and FIR filters etc. Hence we always try for good multiplier architecture to increase the efficiency and performance of a system. Vedic multiplier is one such high speed multiplier architecture. This 'Vedic Mathematics' is the name given to the ancient system of mathematics or, to be precise, a unique technique of calculations based on simple rules and principles, with which any mathematical problem can done with the help of arithmetic, algebra, geometry or trigonometry can be solved. Multiplication plays an important role in the processors. It is one of the basic arithmetic operations and it requires more hardware resources and process ing time than the other arithmetic operations. Vedic mathematic is the ancient Indian system of mathematic. It has a unique technique of calculations based on 16 Sutras. The multiplication sutra between these 16 sutras is the Urdhva Tiryakbhyam sutra which means vertical and crosswise. In this paper it is used for designing a high speed, low power 4*4 multiplier. The proposed system is design using Verilog and it is implemented through Xilinx ISE 12.1.

Keywords: Multiplier, Vedic multiplier, Vedic Mathematics, Urdhava Triyagbhyam.

I. INTRODUCTION

Multiplication is the most important arithmetic operation in signal processing applications and inside the Processor. As speed is always a major requirement in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. Vedic mathematic was reconstructed from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time.

These are the 16 basic sutra of Vedic mathematic:

1) (Anurupye) Shunyamanyat -If one is in ratio, the other is zero.
2) ChalanaKalanabyham -Differences and similarities.
3) Ekadhikina Purvena- By one more than the previous One.
4) Ekanyunena Purvena - By one less than the previous one.

5) Gunakasamuchyah-Factors of the sum is equal to the sum of factors.
6) Gunitasamuchyah-The product of sum is equal to sum of the product.
7) Nikhilam Navatashcaramam Dashatah - All from 9 and last from 10.
8) Paraavartya Yojayet-Transpose and adjust.
9) Puranapuranabyham - By the completion noncompletion.
10) Sankalana- vyavakalanabhyam -By addition and by subtraction.
11) Shesanyankena Charamena- The remainders by the last digit.
12) Shunyam Saamyasamuccaye -When the sum is same then sum is zero.
13) Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam -Vertically and crosswise.
15) Vyashtisamanstih -Part and Whole.
16) Yaavadunam- Whatever the extent of its deficiency.

II. VEDIC SUTRA - URDHWA TIRYAKBHYAM

The 16 Vedic Sutras apply to and cover almost every branch of Mathematics. They apply even to complex problems involving a large number of mathematical operations. Among these sutras, Urdhwa Tiryakbhyam Sutra is the most efficient for performing multiplication. The use of this sutra can be extended to binary multiplication as well .This Sutra translates to “Vertical and crosswise”. It utilizes only logical AND operation, half adders and full adders to perform multiplication where the partial products are generated prior to actual multiplication. This saves a considerable amount of processing time. Moreover it is a robust method of multiplication.

Consider two 8-bit numbers, a (a 8-a1) and b (b8-b1) where 1 to 8 represents bits from the least significant bit to the most significant bit. The final Product is represented by P (P16-P1). In Fig.1, the step by step method of multiplication of two 8-bit numbers using Urdhwa Tiryakbhyam Sutra is illustrated. The bits of the multiplier and multiplicand are represented by dots and the two way arrow represents the logical AND operation between the bits which gives the partial product terms.

In the conventional design of Urdhwa Tiryakbhyam sutra based multiplier, only full-adders and half-adders are used for addition of the partial products. But, the capability of full-adder is limited to addition of only 3 bits at a time.

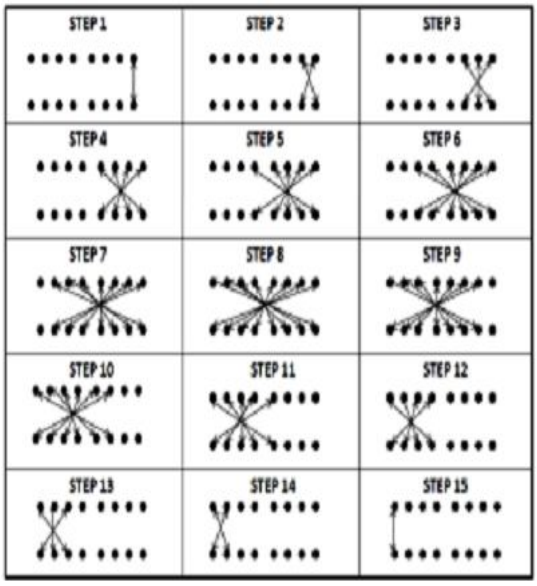

Fig.1. 8-bit binary multiplication using Urdhwa Tiryakbhyam Sutra

So, a large number of stages are required to get the final product. Higher order compressors discussed in next section can be employed to add more than 3 bits at a time (upto 7 bits) and hence can reducethe intermediate stages.

III COMPRESSOR ADDER

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4

or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The compressor adder used here is a 4:2 compressor adder. A comparison of the 4:2 compressor with an equivalent circuit, using full adders and half adders has also been given below.

A. 4:2 Compressor Adder

A 4:2 compressor as shown in fig.3. is capable of adding 4 bits and one carry, in turn producing a 3 bit output. The internal architecture of the same has been show in fig.4. It can be clearly seen, the critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders and half adders. For the sake of comparison, the equivalent circuit to add 5 bits has also been shown in Fig. 5.

Let us consider the propagation delay of a gate to be tp. It is well known that a full adder has a total propagation delay of 2tp and a half adder has a propagation delay of tp. Considering this, the total propagation delay of a 4:2 adder using full adders and half adders can be calculated as 5tp and can be seen in Fig.5. On the other hand, it can be seen from Fig. 4. that the propagation delay of a 4:2 compressor remains only 3tp. Therefore, a lot increase in speed can be recorded in comparison with an equivalent circuit made of full and half adders, proving to be a highly efficient architecture for addition

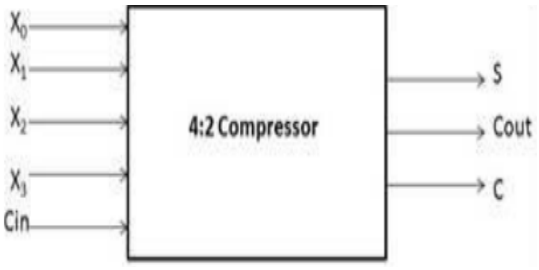

Fig. 3. Black box of a 4:2 compressor adder

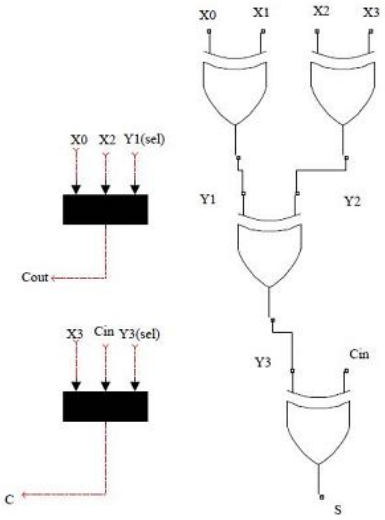

Fig. 4. Gate level diagram of 4:2 Compressors

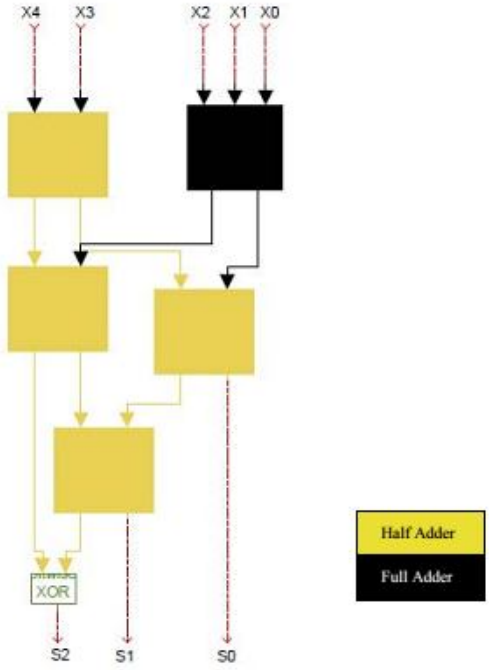

Fig. 5. 4:2 Compressor using full adders and half adders

In order to add more than 5 bits at a time, yet another compressor architecture – the 7:2 compressor adder could be used and this is explained in detail below.

B. 7:2 Compressor Adder

Similar to its 4:2 compressor counterpart, the 7:2 compressor as shown in Fig. 6., is capable of adding 7 bits of input and 2 carry's from the previous stages, at a time. In our implementation, we have designed a novel 7:2 compressor utilizing two 4:2 compressors, two full adders and one half adder. The architecture for the same has been shown in Fig. 7. As mentioned earlier, since the 4:2 compressor shows a significant increase in speed by around 66.6%, utilizing the same in this architecture would improve the efficiency as opposed to a conventional approach of adding nine bits at a time using only full adders and half adders. This leads to a great improvisation in speed of the processor. Through experimentation on a Xilinx Spartan-3e FPGA, it was found that the novel 7:2 compressor adder architecture introduced here is 1.05 times faster than a conventional approach. This result justifies the need of utilizing this compressor in our design.

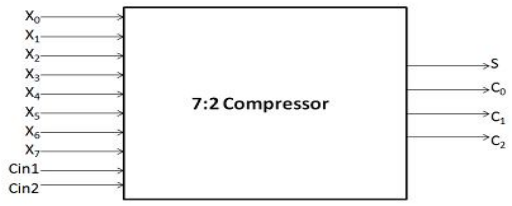

Fig. 6 Black box representation of a 7:2 Compressor Adder

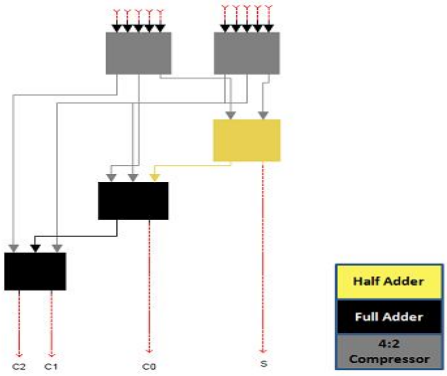

Fig.7 7:2 Compressor using 4:2 Compressor adder

IV. RESULT AND DISCUSSION

The proposed 8-bit multiplier is coded in Verilog HDL, simulated using Xilinx ISim simulator, synthesized using Xilinx XST for Spartan 3E: XC3S500E-4FG320 FPGA and verified for possible inputs given below. Inputs are generated using Verilog HDL test bench. The simulation result for 8-bit multiplier is shown in the Figure 8

Figure 8. Simulation results for various input combinations

Comparison with Various Architectures

The 8-bit multiplier designed is compared with various architectures in terms of total delay, logic delay, route delay and number of logic levels. The results obtained are tabulated in Table I. From table I, it is evident that there is a reduction in both total delay and logic levels. The routing delay is found to be 9.424 ns, the

logic delay is 5.626 ns; thus, giving a total delay of 15.050 ns. The number of logic levels is 11. Thus, it is clear that the proposed design outperforms the other popular multiplier architectures. The proposed architecture can be used to develop a high speed complex number multiplier with reduced delay.

Table I. Comparison between proposed and other architectures

Multiplier Type	Proposed 8-bit multiplier	Normal 8-bit Vedic multiplier	8-bit array multiplier using CSA	8-bit Wallace tree multiplier
Total Delay (ns)	15.050	17.430	17.533	15.969
Logic Delay (ns)	5.626	6.030	6.026	5.823
Route Delay (ns)	9.424	11.400	11.507	10.146
Logic Levels	11	13	13	12

V. CONCLUSION

This paper presents a novel way of realizing a high speed multiplier using Urdhva Tiryagbhyam sutra and carry skip addition technique. A 4-bit modified multiplier is designed. The 8-bit multiplier is realized using four 4-bit Vedic multipliers and modified ripple carry adders. Ripple carry adders are modified because not all bits have same weight and hardware can be reduced by reducing the number of full adders used. Though the number of gates used is fairly high, the increase in speed compensates for the increase in area. The proposed 8-bit multiplier gives a total delay of 15.050 ns which is less when compared to the total delay of any other renowned multiplier architecture. Results also indicate a 13.65% increase in the speed when compared to normal V edic multiplier without carry-skip technique. Our design outshines all other designs.

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