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A Novel Low Power Pulse- Triggered Flip-Flop Design Based on TSPC Latch in FPGA Technology

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Abstract: In this paperwe presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to design in various performance aspects provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligentlyachieved by employing a simple pass transistor. The proposed design successfully solves the long discharging path problem in conventionalexplicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Based on post-layout simulation results using Microwind CMOS 90-nm technology. The best power-delay-product performance in seven FF designs under comparison. Its maximum power saving against rival designs is up to 38.4%.Compared with the conventional transmission gate-based FF design, theaverage leakage power consumption is also reduced by a factor of 3.52Keywords: Booth encoder, computer arithmetic, digital signal processing, spurious power suppression technique, low power.
Keywords: MOSFET, Pulse triggered flip flop, universal shift registers, low power, delay, power delay product

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design [1], [2].

Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit [6]. In an implicit-type P-FF, the pulsegenerator is a built-in logic of the latch design, and no explicit pulsesignals are generated. In an explicit-type P-FF, the designs of pulsegenerator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. Thisis because the former merely controls the discharging path while thelatter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, whichleads to inferior timing characteristics. The situation deteriorates further when low-power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mappingare applied [7]–[10]. As a consequence, the transistors of pulse generation logic are often enlarged to assure that the generated pulses aresufficiently wide to trigger the data capturing of the latch. Explicit-typeP-FF designs face a similar pulse width control issue, but the problemis further complicated in the presence of a large capacitive load, e.g., when one pulse generator is shared among several latches.

Existing Pulse Triggered Flip Flop:

An explicit type pulse triggered structure and a modified true single phase clock latch based on a signal feed through scheme as shown in Fig a.

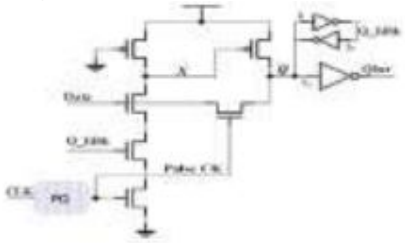

Fig a:Existing pulse triggered flip flop

The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved byemploying a simple pass transistor. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor and the delay can be greatly shortened.

In this paper, we will present a novel low-power implicit-type P-FFdesign featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of aslight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layoutarea is even slightly reduced. This gives rise to competitive power andpower–delay–product performances against other P-FF designs.

II. PROPOSED P-FF DESIGN

The proposed system is designed with signal feed through scheme without feedback circuits that is only capable of designing the sequential circuits that does not have feedback operation as shown in Fig. Added to the pass transistor in the existing system, a pMOS transistor is used controlled by clock signal to reduce power.

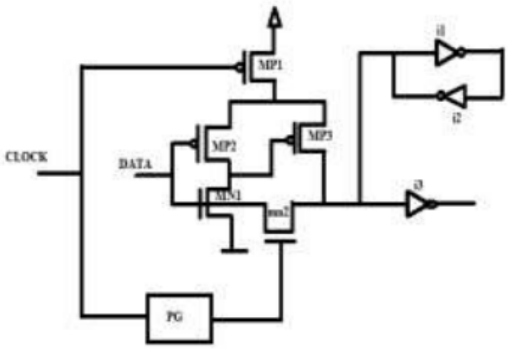

Fig b: Proposed Pulse Triggered Flip Flop

Universal Shift Register

A universal shift register is an integrated logic circuit that can transfer data in three different modes designed using pulse triggered flip flop as shown in the Fig c. Like a parallel register it can load and transmit data in parallel. Like shift registers it can lo ad and transmit data in serial fashions, through left shifts or right shifts. In addition, the universal shift register can combine the capabilities of both parallel and shift registers to accomplish tasks that neither basic type of register can perform on its own.

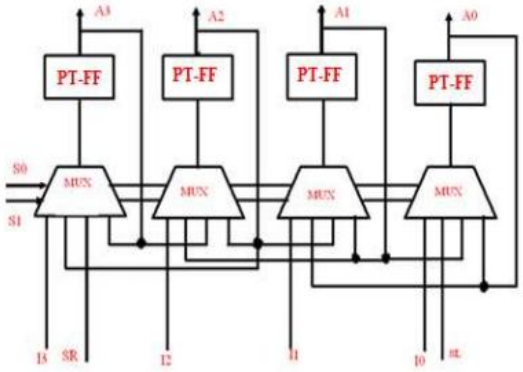

Fig c: Universal Shift Register

A. Conventional Implicit-Type P-FF Designs

A state-of-the-art P-FF design, named ip-DCO, is given in Fig. 1(a)[6]. It contains anANDlogic-based pulse generator and a semi-dynamicstructured latch design. Inverters I5 and I6 are used to latch data andinverters I7 and I8 are used to hold the internal node . The pulse generator takes complementary and delay skewed clock signals to generatea transparent window equal in size to the delay by inverters I1-I3. Twopractical problems exist in this design. First, during the rising edge,nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to alarge switching power. The other problem is that node controls twolarger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

Fig. 1(b) shows an improved P-FF design, named MHLLF, by employing a static latch structure presented in [11]. Node is no longerprecharged periodically by the clock signal. A weak pull-up transistorP1 controlled by the FF output signal Q is used to maintain the nodeX level at high when Q is zero. This design eliminates the unnecessary discharging problem at node . However, it encounters a longerData-to-Q (D-to-Q) delay during “0” to “1” transitions because node X is not pre-

discharged. Larger transistors N3 and N4 are required toenhance the discharging capability.

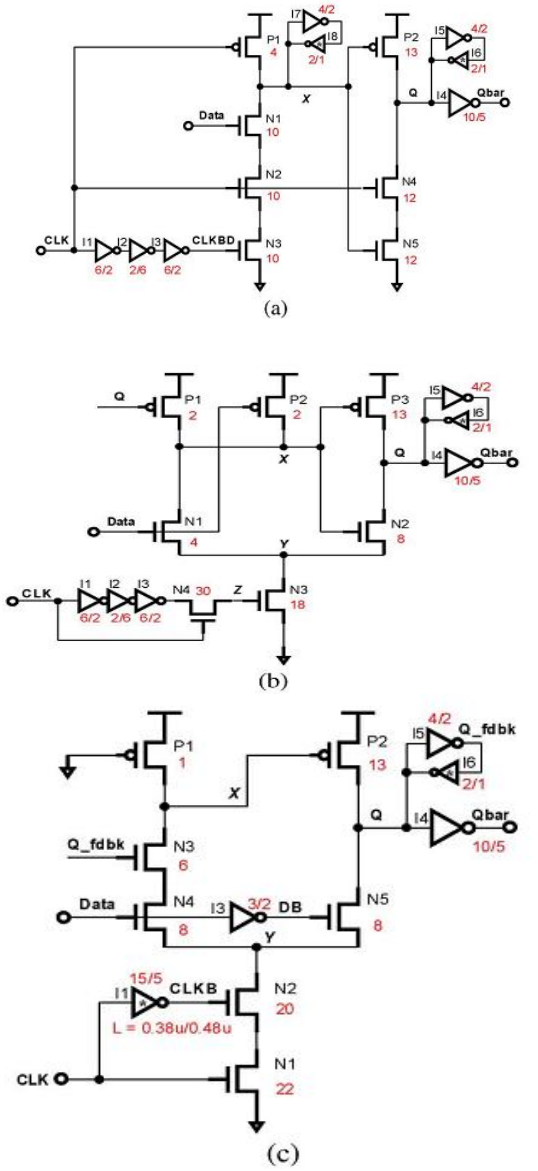

Fig. 1. Conventional P-FF designs.
(a) ip-DCO . (b) CDFF.
(c) SCCER

1)ip-DCO: ip-DCO is known as the implicit data close to output. It is an implicit type flip-flop. In this method the pulse is generated inside the flip-flop. A state-of-the-art P-FF design, named ip-DCO, is given in Fig.1. It contains an AND logic based pulse generator and a semi-dynamic structured latchdesign. Semi-Dynamic Flip-Flop is a high performance flipflop because of its small delay and simple topology. It is measured to be one of fastest flip-flops today. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 areturned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power.

2)MHLFF: The modified hybrid latch flip-flop is known as MHLFF and this is an type of implicit type flip-flop. MHLFFshows an improved P-FF design in fig.2. It employs a static latch structure. A static latch can remember as long as gate power is supplied. It uses feed-back to remember, rather than depending on the charge on a capacitor. Node X is no longerprecharged periodically by the clock signal. A weak pull-uptransistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero. This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data -to-Q (D-to-Q) delay during "0" ,"1" transition because node is not predischarged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact"1".

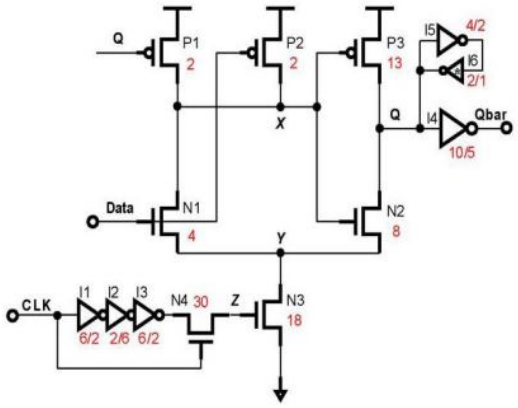

Fig.2. MHLFF

*3)SCCER:*SCCER is known as the single ended conditional capturing energy recovery P-FF.It is a refined low power PFF design using a conditional discharged technique. This technique is also used to present a new flip -flop ConditionalDischarge flip-flop (CDFF). CDFF use a pulse generator which is suitable for double edge sampling. CDFFhas two stages. First is responsible for capturing the Low-to-High transition and second stage captures the High-to-Low input transition. In this SCCER design, the keeper logic is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node. The discharge pathcontains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node, an extranMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high.

The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series,i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed toensure node can be properly discharged. This implies wider N1and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

B. Proposed P-FF Design

Recalling the four circuits reviewed in Section II-A, theyall encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. 2(a), the proposed design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed designdistinct from the previous one. First, a weak pull-up pMOS transistor MP1.

In SCCER design, the discharge control signal is driven by asingle transistor. Parallel conduction of two nMOS transistors (N2and N3) speeds up the operations of pulse generation. Thus the number of stacked transistors along the discharging path isreduced. To enhance the discharging condition, transistor P3 is added. When the FF output Q changes from 0 to 1 the conditional pulse enhancement technique effectively takesplace. Thus this leads to the better power performancecompared to the indiscriminate pulse enhancement approach.

The post layout simulations on various P-FF were conducted to obtain the performance figure of the proposed design. These designs include three flip-flops namely ip-DCO, MHLFF and SCCER. And those designs are discussed above. The target technology is the UMC 90-nm CMOS process. The operating Condition used in simulations is 500 MHz/1.0V.

III. SIMULATION RESULTS

The simulation results of above designs are shown below in the Fig. 5 to Fig. 8.

The power consumed by the ip-DCO is 134.34mW, MHLFF is 120.74mW, SCCER is 68.32mW and P-FF is 55.3mW.Bycomparing the above results, we came to know that power consumption of P-FF design is low.

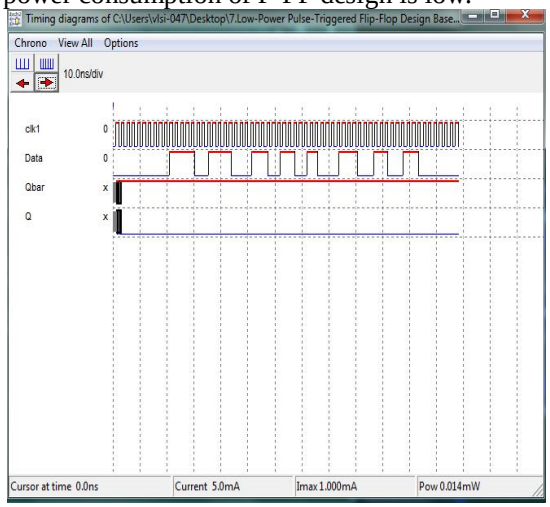

Fig.3. Power consumed by ip-DCO

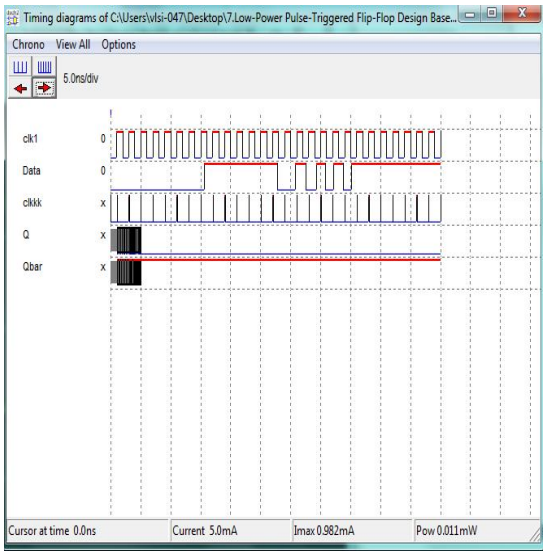

Fig.4. Power consumed by MHLFF

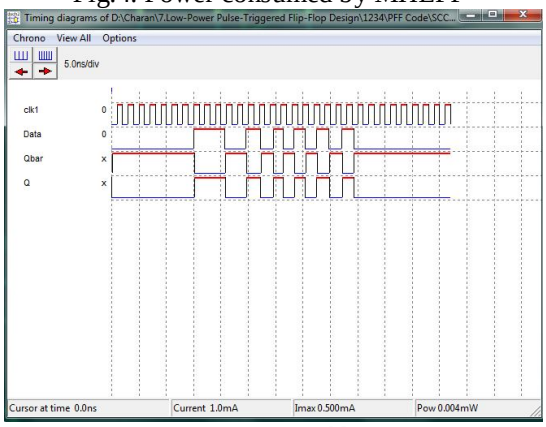

Fig.5. Power consumed by SCCER

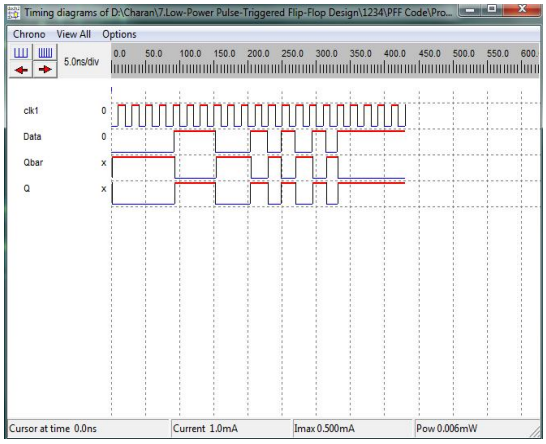

Fig.6. Power consumed by P-FF

Table. I. Power Comparison

FF	TOTAL ESTIMATED POWER CONSUMPTION P(mW)
ip- DCO	134.34
MHLFF	120.74
SCCER	68.32
P-FF	55.3

CONCLUSIONS

In this paper, we devise a novel low-power pulse-triggered FFdesign. This was successfully done by reducing the number oftransistors stacked along the discharging path by incorporatinga PTL-based AND logic. The table 1 has been added to verify that the proposed design will be better compared to the exi sting design like ip-DCO, MHLLF, SCCER.
The pulse triggered flip flop based on signal feed through scheme is used to design universal shift registers. The universal shift registers are designed using existing and proposed pulse triggered flip flop using CMOS design with nanometer Technology to achieve low power, less delay and power delay product.

REFERENCES

[1] H. Kawaguchi and T. Sakurai, “A reduced clock-swing flip-flop(RCSFF) for 63% power reduction,”IEEE J. Solid-State Circuits, vol.33, no. 5, pp. 807–811, May 1998.
[2] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, “A novel highspeed sense-amplifier-based flip-flop,”IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 11, pp. 1266–1274, Nov. 2005.
[3] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper,“Flow-through latch and edge-triggered flip-flop hybrid elements,” in IEEE Tech. Dig. ISSCC, 1996, pp. 138–139.
[4] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta,R. Heald, and G. Yee, “A new family of semi-dynamic and dynamic flipflops with embedded logic for high-performance processors,”IEEEJ.Solid-State Circuits, vol. 34, no. 5, pp. 712–716, May 1999.

[5] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J.Sullivan, and T. Grutkowski, "The implementation of the Itanium 2microprocessor,"IEEE J. Solid-State Circuits, vol. 37, no. 11, pp.1448–1460, Nov. 2002.
[6] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De,"Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," inProc. ISPLED, 2001, pp. 207–212.
[7] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction,"IEEE J. Solid-State Circuits, vol. 36, no. 8, pp.1263–1271, Aug. 2001.
[8] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional prechargetechniques for power-efficient dual-edge clocking," inProc. Int. Symp.
Low-Power Electron. Design, Monterey, CA, Aug. 12–14, 2002, pp.56–59.
[9] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and lowpower conditional discharge flip-flop,"IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May 2004.
[10] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki,"Conditional data mapping flip-flops for low-power and high-performance systems,"IEEE Trans. Very Large Scale Integr. (VLSI) Systems,vol. 14, pp. 1379–1383, Dec. 2006.
[11] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani,"Low power single- and double-edge-triggered flip-flops for high speed applications,"Proc. Inst. Electr. Eng.—Circuits Devices Syst., vol. 152,no. 2, pp. 118–122, Apr. 2005.
[12] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra lowpower clocking scheme using energy recovery and clock gating,"IEEETrans. Very Large Scale Integr. (VLSI) Syst., vol. 17, pp. 33–44, Jan.2009.
[13] P. Zhao, J. McNeely, W. Kaung, N. Wang, and Z. Wang, "Design ofsequential elements for low power clocking system,"IEEE Trans. VeryLarge Scale Integr. (VLSI) Syst., to be published.
[14] Y.-H. Shu, S. Tenqchen, M.-C. Sun, and W.-S. Feng, "XNOR-baseddouble-edge-triggered flip-flop for two-phase pipelines,"IEEETrans.Circuits Syst. II, Exp. Briefs, vol. 53, no. 2, pp. 138–142, Feb. 2006.
[15] V. G. Oklobdzija, "Clocking and clocked storage elements in a multigiga-hertz environment,"IBM J. Res. Devel., vol. 47, pp. 567–584, Sep.2003.