INTERNATIONAL JOURNAL OF RESEARCH
In Advanced Engineering Technologies

Volume 5, Issue 1 SEP 2015

Data Encoding Techniques for Low Power Consumption in Network-on-Chip

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***Abstract*—** An ever more significant fraction of the overall power dissipation of a network-on-chip (NoC) based system on-chip (SoC) is due to the interconnection system. In fact, as technology shrinks, the power contribute of NoC links starts to compete with that of Noc routers. In this paper, we propose the use of data encoding techniques as a viable way to reduce both power dissipation and energy consumption of Noc links. The proposed schemes are general and transpent with respect to the fundamental Noc structure. Experiments carried out on both synthetic and real traffic scenarios shows that the efficiency of the proposed schemes, allows to save power without any degradation in the performance.

Index Terms-Coupling switching activity, data encoding, interconnection on chip, low power, network-on-chip (Noc), power analysis.

INTRODUCTION: As the number of cores integrated into a system on-chip (SoC) increases, the role played by the interconnection system becomes more and more important. The International Technology Roadmap for Semi-conductors depicts the on-chip communication issues as one of the limiting factors for performance and power consumption in current and next generation SoCs. Design in the era of ultra deep submicron silicon is mainly dominated by issues concerning the communication infrastructure. As the design complexity increases, the total length of the interconnection wires increases, resulting in long transmission delay and higher power consumption. In addition, the distance between wires shrinks with technology, increasing coupling capacitance, and the height of the wire material increases resulting in greater fringe capacitance. Now a days it is widely recognized that network-on-chip (NoC) architectures represent the most viable solution to cope up with scalability issues of many-core systems, in future to meet the performance, power, and reliability requirements which characterize future ambient intelligent applications. The importance of interconnects in complex many of the core chips has out run the importance of transistors as a dominant factor of performance, power, cost, and reliability. Sophisticated on-chip communication protocols, involving advanced adaptive routing algorithms, selection policies, data protection schemes, and mechanisms aimed at guaranteeing the quality-of-service are pushing the interconnect system to become one of the main elements which characterizes the system in terms of both power dissipation and energy consumption.

Overview of the proposal: The power dissipated by the links of Network-On- Chip (NoC) is very high when compared to other elements of communication system namely routers , and the network interfaces NI's . Aim of this paper is to reduce power consumption in the links. The Main aim of this paper is to

reduce the power consumption in network on chip by reducing number of transitions from 0 to1 or 1 to 0.To achieve this we are proposing three encoding schemes. In each scheme we will try to reduce the number of transition types. So that the energy required for transition can be reduced. The main goal of the proposed encoding scheme is to reduce the power dissipation by minimizing the coupling transition activities on the links of the interconnection network. In this paper three sets of encoding schemes are discussed.

Block diagram:

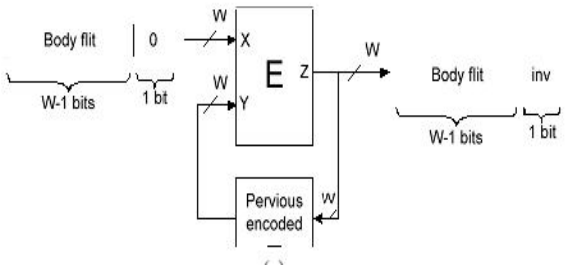

Fig.1.Block diagram of Encoder

Description of the block diagram

In Encoder side according to our encoding scheme the logic block E changes. W is the length of the input data. X is the input data and Y is previous output of the encoder. It is connected to logic block E through feedback. The bit inv contains the information regarding type of inversion to be done. The block diagram of encoder is shown in fig.1.

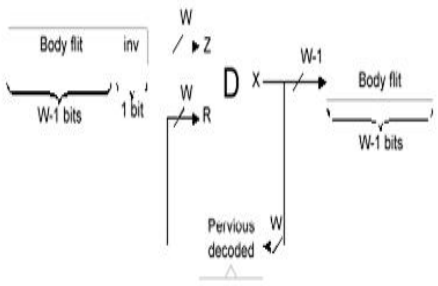

Fig.2.Block diagram of Decoder

In Decoder side according to our schemes logic block D changes for all three schemes. As it is the inversion to the decoder Input to the decoder D is the output of the encoder. R represents the previous output of the decoder logic block D. R is a feedback signal to the input of the decoder. Z contains inv bit which contains the information regarding type of inversion. Based on the inv bit the logic block D will perform the appropriate inversion to the incoming data Z to get the original information. The block diagram of decoder is shown in fig.2.

PROPOSED ENCODING SCHEMES

Scheme I: The aim of this scheme is to reduce the number of type1 and type II transitions. The present data is compared with the previous data. The Encoder E in fig.1 decides whether the inversion is necessary for the present data or not.

Time	Normal			Odd Inverted		
	Type I			Type II, III and IV		
t – 1 t	00, 11 10, 01	00, 11, 01, 00 01, 10, 00, 11	01, 10 11, 00	00, 11 11, 00	00, 11, 01, 10 00, 11, 01, 10	01, 10 10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
t – 1 t	Type II 01, 10 10, 01			Type I 01, 00 11, 00		
t – 1 t	Type III 00, 11 11, 00			Type I 00, 11 10, 01		
t – 1 t	Type IV 00, 11, 01, 10 00, 11, 01, 10			Type I 00, 11, 01, 10 01, 10, 00, 11		

Table1: Encoding Using Odd Inversion

Power model: If the flit is odd inverted before being transmitted, the dynamic power on the link is

$P' \propto T'0 \rightarrow 1 + (K1T'1 + K2T'2 + K3T'3 + K4T'4)Cc$ (1)

$Ty > (W-1)/2$ (2)

This represents the condition used to determine the odd inversion has to be performed or not.

Proposed Encoding Architecture: The proposed encoding architecture which is based on odd invert condition is defined by (2), the internal view of the encoder is shown in fig 3.

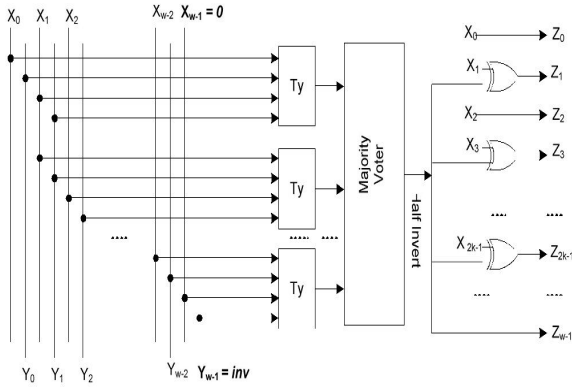

Fig.3. Internal view of the encoder block (E)

As said earlier the type I and type II transitions are reduced.TypeI means only one bit is changed keeping the other bit constant.TypeII transition means changing the both bits i.e. from high to low and low to high. The Ty block in E compares the present data with the previous data. The output of Ty block is either 0 or 1.If type1 and type11 transitions are present then the out of Ty block is 1 otherwise output is 0.T given to the output of Ty block is to the majority voter. The majority voter verifies the condition for odd inversion given by 2.

Scheme II: Scheme 11 making use of both the odd inversion and full inversion. This full inversion operation converts the type 11 transitions to type 1v transitions. The block diagram for scheme11 is same as scheme1 but the only encoder E varies. The operation of circuit diagram of scheme11 is same Expect the internal logic of encoder.

1) Power Model: Let us indicate with *P, P',* and *P''* the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, and full inversion, respectively. The odd inversion leads to power reduction when $P' < P''$ and $P' < P$. The power P'' is given by [23]

$P'' \propto T1 + 2T4^{**}$ (3)

Neglecting the self-switching activity, we obtain the condition $P' < P'' \; T2 + T3 + T4 + 2T1^{***} < T1 + 2T4^{**}$ (4)

Therefore, we can write

$2(T2 - T4^{**}) < 2Ty - w + 1$ (5)

The odd inversion condition is obtained as

$2(T2 - T4^{**}) < 2Ty - w + 1$

$Ty > (w - 1)/2$ (6)

Similarly, the condition for the full inversion is obtained from $P'' < P$ and $P'' < P'$. The inequality $P'' < P$ is satisfied.

$T2 > T4^{**}$ (7)

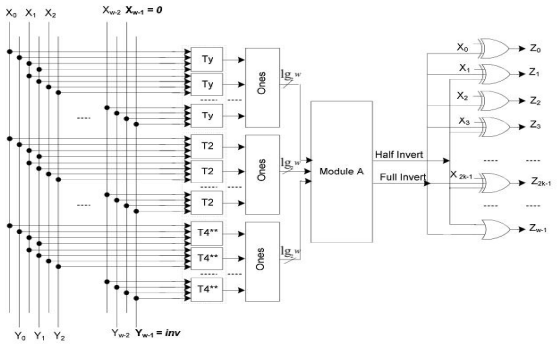

Fig.4. Encoder architecture Scheme II

Internal view of Encoder of scheme 11:In addition of Ty block which is given in scheme 1 we have T2 and T4 ** blocks, which includes the first stage. The second stage is formed by a set of 1's blocks, it counts the number of 1"s in its inputs. The output of these ones block has

with of log2w which is indicated in the fig.4.the output of the ones block which is on the top determines the number of transitions that odd inverting of pair bits leads to the reduction of the link power. The ones block which is in middle identifies the number of transitions whose full inverting of pair bits lead to the link power reduction. Thus the ones block which is at the last specifies the number of transitions whose full inverting of pair bit leads to the increased link power. Based on the number of 1"s for each transition type, Module A decides whether the odd inversion or full inversion operation should be performed for the low power consumption.

For this module, if either the (2) or (7) should be satisfied. If it satisfies the corresponding output signal will become'1'.In case no invert operation should be taken place, then none of the output is set to'1'.

Scheme III: In the proposed encoding Scheme III, we add even inversion to Scheme II. The reason is that odd inversion converts some of Type (T1 ∗∗∗) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions indicated as T1∗∗/T1∗∗∗in the table is converted to Type IV/Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the previous one to decide whether odd, even, full, or no inversion of the current data can give rise to the link power reduction.

Time	Normal			Even Inverted		
	Type I			Type II, III and IV		
t – 1 t	01, 10 00, 11	00, 11, 01, 10 01, 10 10, 01, 11, 00	01, 10 11, 00	01, 10 10, 01	00, 11, 01, 10 00, 11, 01, 10	00, 11 11, 00
	T1*	**T1****	**T1*****	**Type II**	**Type IV**	**Type III**
t – 1 t	**Type II** 01, 10 10, 01			**Type I** 01, 00 00, 11		
t – 1 t	**Type III** 00, 11 11, 00			**Type I** 00, 11 01, 10		
t- 1 t	**Type IV** 00, 11, 01, 10 00, 11, 01, 10			**Type I** 00, 11, 01, 10 10, 01, 11, 00		

Table2: Encoding Using Even Inversion

Power Model: Let us indicate with *P'*, *P''*, and *P'''* the power dissipated by the link when the flit is transmitted with no inversion, odd inversion, full inversion, and even inversion, respectively.

The even inversion leads to power reduction when $P'''< P$, $P'''< P'$, and $P'''< P''$. we obtain

$$Te> (w-1)/2,\ Te > Ty,\ 2T2 - T4^{**} < 2Te - w+1. \quad (8)$$

The full inversion leads to power reduction when $P'''< P$, $P'''< P'$, and $P'''< P''$. Therefore, the full inversion condition is obtained as

$$2\,(T2 - T4^{**}) > 2Ty - w + 1, \quad (T2 > T4^{**})$$

$$2\,(T2 - T4^{**}) > 2Te - w + 1. \quad (9)$$

Similarly, the condition for the odd inversion is obtained from $p' < P$, $P' < P''$ and $p'<p'''$. The odd inversion condition is satisfied when

$$2\,(T2 - T4^{**}) < 2Ty - w + 1,\ Ty > (w-1)/2$$

$$Te< Ty \quad (10)$$

When none of the equations is satisfied, no inversion will be performed.

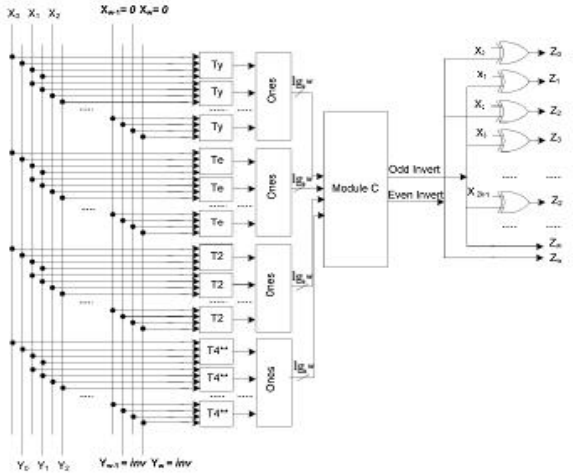

Fig. 5 Encoder architecture for Scheme III.

Proposed Encoding Architecture: The operating principles of this encoder are similar to those of the encoders implementing Schemes I and II. The proposed encoding architecture, which is based on the even invert condition ,the full invert condition, and the odd invert condition of, is shown in Fig. The *w*th bit of the previously encoded body flit is indicated by inv which shows if it was even, odd, or full inverted (inv = 1) or left as it was (inv = 0).Similar to the procedure used to design the decoder for scheme II, the decoder for scheme III may be designed.

RESULTS

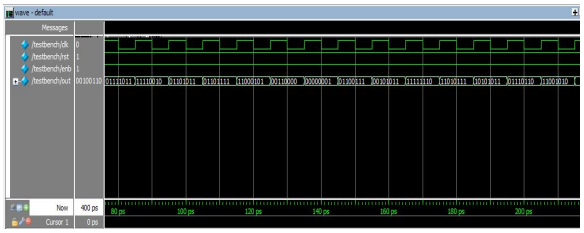

Fig .6 Simulation results of Scheme I

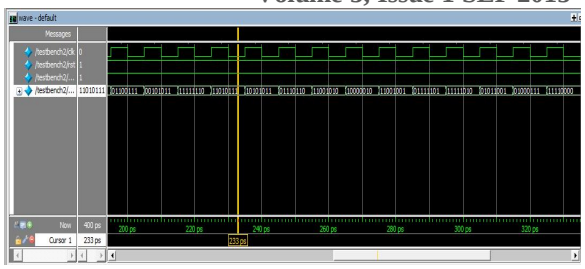

Fig.7 Simulation results of scheme II

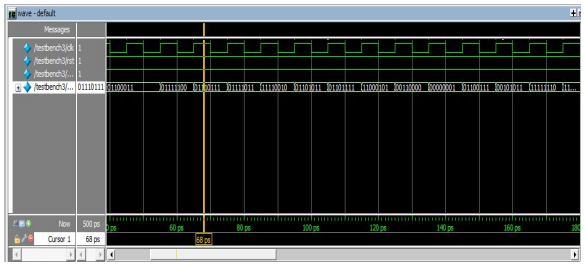

Fig.8 Simulation results of scheme III

Power report:

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	1.089	1	--	--
Logic	0.247	66	1920	3.4
Signals	0.811	103	--	--
IOs	48.858	11	66	16.7
BRAMs	0.055	1	4	25.0
Total Quiescent Power	0.068			
Total Dynamic Power	52.019			
Total Power	52.087			

Fig.9 Power report of schemeI

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.661	1	--	--
Logic	0.136	24	1920	1.3
Signals	0.322	62	--	--
IOs	49.040	11	66	16.7
BRAMs	0.056	1	4	25.0
Total Quiescent Power	0.068			
Total Dynamic Power	51.174			
Total Power	51.242			

Fig.10 Power report of schemII

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.713	1	--	--
Logic	0.271	22	1920	1.1
Signals	0.734	60	--	--
IOs	48.394	11	66	16.7
BRAMs	0.056	1	4	25.0
Total Quiescent Power	0.068			
Total Dynamic Power	51.127			
Total Power	51.195			

Fig.11 Power report of schemeIII

Delay comparision:

Methods used	Delay(ns)
Data Encoding Scheme I	4.642
Data Encoding Scheme I I	3.899
Data Encoding Scheme I I I	3.286

Table3:Delay comparision

Time comparision :

Methods used	Minimum period	Minimum output required time after clock	Minimum output required time after clock
Data Encoding Scheme I	4.642 ns	4.339 ns	4.063 ns
Data Encoding Scheme II	3.899 ns	4.377 ns	4.040 ns
Data Encoding SchemeIII	3.286 ns	4.334ns	4.040 ns

Table4.Time comparision

CONCLUSION

In this paper, a set of new data encoding schemes aimed at reducing the power dissipated by the links of NoC are presented. In fact, links are responsible for a significant fraction of the overall power dissipated by the communication system. In addition, their contribution is expected to increase in future technology nodes. As compared to the previous encoding schemes proposed in the literature, the reason behind the proposed schemes is to minimize not only the switching activity, but also the coupling switching activity which is mainly responsible for link power dissipation in the deep sub micron meter technology regime. The proposed encoding schemes are agnostic with respect to the underlying NoC architecture in the sense that their application does not require any modification neither in the routers nor in the links. An extensive evaluation has been carried out to assess the impact of the encoder and decoder logic in the NI. Overall, the application of the proposed encoding schemes allows savings up to 51% of power dissipation and 14% of energy consumption without any significant performance degradation .

FUTURE WORK

To implement efficient scheme III with GRAY code & prove its efficiency through hardware synthesis. In order to increase the throughput rate grouping rate will be increased. To analyze the trade off between complexity Vs. power reduction.

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