INTERNATIONAL JOURNAL OF RESEARCH
In Advanced Engineering Technologies

Volume 4, Issue 5 AUG 2015

Study of Unbalance Dc-Link Voltage in A Seven Level Phase Shifted Modulated MLCI For EV Traction Motor Drive

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ABSTRACT- - **to amass balanced line-to-line output voltages, this paper proposes a pulse breadth modulation PWM strategy and within the vary of linear modulation to maximise the modulation index wherever the output voltage will be linearly adjusted within the construction cascaded electrical converter (MLCI) operational underneath unbalanced dc-link conditions. underneath these conditions linear modulation index is reduced as reference voltage will increase effecting output voltage imbalance. These effects square measure analyzed by the voltage vector area for MLCI is evaluated very well. From this analysis, the idea behind the output voltage imbalance is explained, and also the most linear modulation vary considering AN unbalanced dc-link condition is evaluated. Neutral voltage modulation is planned to realize output voltage equalization furthermore on extend the linear modulation vary up to the most accessible purpose in theory. within the planned technique, overlarge of a dc-link imbalance precludes the equalization of the output voltages. This limitation is additionally mentioned. The simulations for AN 7-level phase-shifted modulated. MLCI for electrical vehicle traction motor drive show that the planned technique is ready to balance line-to-line output voltages furthermore on maximize the linear modulation vary underneath the unbalanced dc-link conditions.**

Index Terms—**Harmonic injection, multilevel cascaded inverters (MLCIs), neutral voltage modulation (NVM), phase-shifted (PS) modulation, space vector pulse width modulation (SVPWM).**

I. INTRODUCTION

THE development of electrical and hybrid-electric vehicles can supply several new opportunities and challenges to the facility industry, particularly within the development of the most traction motor drive. several current and future styles can incorporate the employment of induction motors because the primary supply for traction in electrical vehicles. styles for significant duty trucks and lots of military combat vehicles that have giant electrical drives would force advanced power electronic inverters to satisfy the high power demands (>250 kW) needed of them [5]. Development of electrical drive trains for these giant vehicles can end in accumulated cell potency, lower emissions, and certain higher vehicle performance (acceleration and braking). construction

inverters square measure unambiguously fitted to this application as a result of the high VA ratings doable with these inverters. With the construction inverters with reference to curving output voltages may be obtained from many steps of voltages. construction inverters posses low dv/dt characteristics, low harmonics within the output voltage and current and therefore the switch of terribly high voltages may be achieved by stacking construction electrical converter modules [1]–[5]. For this reason, construction inverters are applied in numerous application fields [6]–[10]. Among numerous topologies for construction inverters, the construction cascaded electrical converter (MLCI) structure is one in all the outstanding topologies as a result ofof its easy structure for modularization and fault-tolerant capability.

Therefore, MLCIs square measure used as dynamic voltage trained worker, static synchronous compensator (STATCOM), high-voltage energy memory device, electrical phenomenon inverters, medium-voltage drives, electrical vehicle (EV) traction drives, so on [7]–[9].To achieve superior management a modulation strategy must generate gating signals.

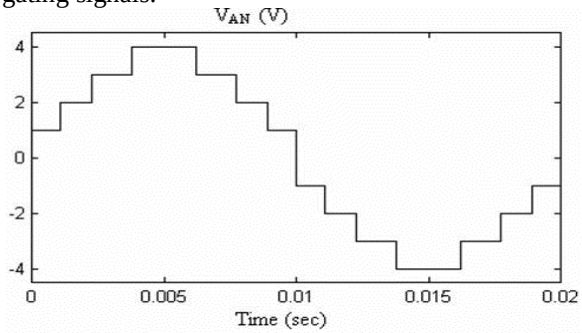

Fig 1 proposed 7-level output

Inverters have been applied in regarding this issue, many studies have been conducted, and they are roughly categorized into multilevel selective harmonic elimination pulse width modulation (PWM) (SHEPWM), multilevel carrier-based PWM, and multilevel space vector PWM (SVPWM) methods. Generally, a carrier-based PWM or SVPWM is preferred in applications such as motor drives, where dynamic properties are very important, whereas SHEPWM is preferred in some high- power static power conversion applications. An SVPWM method has been studied to cover the over modulation range in the multilevel inverter.

A multilevel SVPWM has been proposed in [3] to reduce common-mode voltage. In [4], for the implementation of SVPWM in MLCI series SVPWM method has been reported. In [5], to improve an SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency.

MLCIs requires separate DC sources, if any fault appears in each DC-link or if voltage magnitudes of the DC-link are unequal then output voltage of MLCIs can be unbalanced without proper compensation. To resolve this issue, the available modulation index is reduced under faulty conditions on switch modules in multilevel inverters, and compensation algorithms are proposed for phase-disposition PWM and phase-shifted (PS) PWM cases. For a STATCOM application, a zero sequence voltage to decouple a three-phase MLCI into three single-phase MLCIs is applied as well as zero average active power techniques to operate the MLCI under unbalanced source or load conditions [7]. Reference [8] covers why the optimum angles and modulation indexes are necessary to obtain maximum balanced load voltages in the MLCI when undergone a fault on switching modules.

In [9], a duty cycle modification method has been proposed to compensate an output voltage imbalance caused by single-phase power fluctuations. Reference has shown that a zero sequence component helps to obtain the maximum balanced output voltages in a fault condition. In [10], an offset voltage injection technique is studied to balance the output voltage of the MLCI, but with the use of an integrator in the compensation method may affect the dynamic characteristics in applications such as EV motor drives. Recently, the multilevel multiphase feed forward space vector modulation technique called MFFSVM is proposed to compensate the voltage imbalances in MLCIs.

In this paper, to attain balanced line-to-line output voltages, this paper proposes a pulse width modulation PWM strategy and in the range of linear modulation to maximize the modulation index where the output voltage can be linearly adjusted in the multilevel cascaded inverter (MLCI) operating under unbalanced dc-link conditions. Under these conditions linear modulation index is reduced as reference voltage increases effecting output voltage imbalance. These effects are analyzed by the voltage vector space for MLCI is evaluated in detail. From this analysis, the theory behind the output voltage imbalance is explained, and the maximum linear modulation range considering an unbalanced dc-link condition is evaluated.

Neutral voltage modulation is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in theory. After that, a neutral voltage modulation (NVM) strategy is proposed to achieve output voltage balancing as well as to extend the linear modulation range up to the maximum reachable point in theory. In the proposed method, the neutral voltage reference, which considers a zero sequence voltage to compensate the output voltage imbalance, and an offset voltage to extend the linear modulation range are easily obtained through simple arithmetic calculations. In the proposed method, too large of a dc-link imbalance precludes the output voltages from being balanced. This limitation is also discussed.

In addition, a fault-tolerant operation is naturally covered, because the MLCI undergoing an unbalanced dc-link condition can be considered as an MLCI operating under a faulty condition on switch modules. Compared to the existing methods, the proposed strategy is very simple to implement, compensates the output voltage imbalance in real time, and maximizes the voltage utilization of the dc links. Therefore, if this scheme is applied to applications such as EV traction drive systems, the dynamic characteristics can be greatly improved.

This paper is organized as follows. In Section II, the voltage vector space for the one-by-three configuration MLCI is analyzed for a conceptual study. The proposed modulation strategy for extention7-level is addressed in Section III. In Sections IV the simulations results on the two-by-three MLCI for 7-level are presented. Section V concludes this paper. The output response for 11-level output as shown in Fig.1

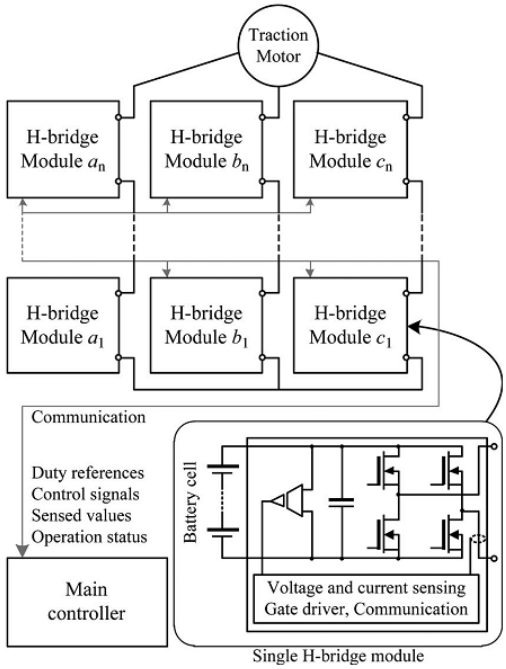

Fig. 2. MLCI-based inverter for EV traction drive.

II. CONFIGURATION FOR MLCI AND VOLTAGE VECTOR SPACE ANALYSIS

A. MLCI CONFIGURATION FOR APPLICATION OF EV TRACTION MOTOR DRIVE

The EV traction motor drive system that is dealt with in this paper is shown in Fig. 2. By configuring the number of the single H-bridge modules various power ratings can be easily implemented for EV, full-size sedan. Each H-bridge involves voltage and current sensing circuitries, gate drivers, and communication interfaces between the module itself and the main controller. For option battery cells can also be included in the H-bridge module. Between two switching legs in the H-Bridge uni-polar modulation technique is implemented.

In addition, battery cells can be also included in the H-bridge module. The uni-polar modulation technique is applied between two switching legs in the H-bridge module. For effective switching in each H-bridge module the applied switching frequency is twice the carrier frequency. PS modulation technique is also used to implement interleaving and multilevel operation to 11-level output. Finally, the effective switching frequency f_{sw} in a phase is

$$f_{sw} = 2N \times f_c \quad \text{------ (1)}$$

Where N = No. of H-bridge modules;

f_c = carrier frequency of PWM

As an example, the carriers for each module, the duty cycles in uni-polar modulation, and the output voltage when N=2 is shown in Fig. 3.

B. VOLTAGE VECTOR SPACE ANALYSIS

The output voltage v_{pn} has three states, i.e., V_{dc} , 0, and $-V_{dc}$, When the dc-link voltage of a single H-bridge module is V_{dc}.

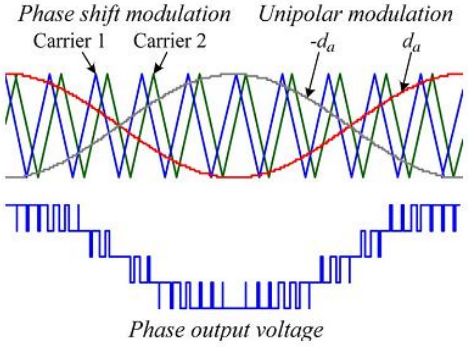

Fig. 3. Unipolar and phase shift modulation for single H-bridge module.

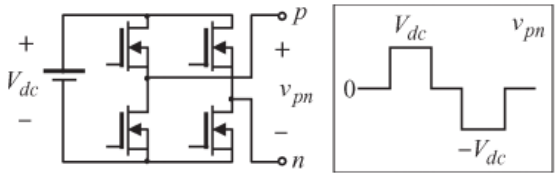

Fig. 4. Output voltage of a single H-bridge module.

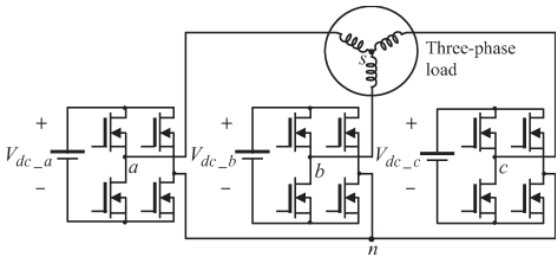

Fig. 5. One-by-three configuration MLCI.

as shown in Fig. 4. By adopting the concept of a switching function, it can be represented as

$$v_{pn} = S_p V_{dc}$$
$$S_p \epsilon \{-1,0,1\}_{p=a,b,or,c} \quad \text{------- (2)}$$

Where S_p = switching function; p =a, b, or c, the phases with two neutral points *s* and *n*. Fig. 5 shows a simple one-by-three configuration MLCI. For more levels from voltage vector space analysis, the main concept is derived from this simple topology. The pole voltages (V_{an},V_{bn},V_{cn}) is defined as voltage between each phase and neutral point *n* and the phase

Voltages (v_{as}, v_{bs}, v_{cs}) are the voltage between the output point of each phase and the load side neutral points. The phase voltages includev_{as},v_{bs}, and v_{cs}. By using this concept, the voltage between the two neutral points is defined as v_{sn} and can be written as

$$v_{sn} = -v_{as} + v_{an} = -v_{bs} + v_{bn} = -v_{cs} + v_{cn} \quad \text{------ (3)}$$

By using the condition that the sum of all phase voltages is zero because the load does not have a neutral line,$V_{sn}$is rewritten as
Under the absence of neutral line at the load, that the sum of all phase voltages is zero,$V_{sn}$is rewritten as

$$v_{sn} = -\frac{1}{3}(v_{an} + v_{bn} + v_{cn}) \quad \text{------- (4)}$$

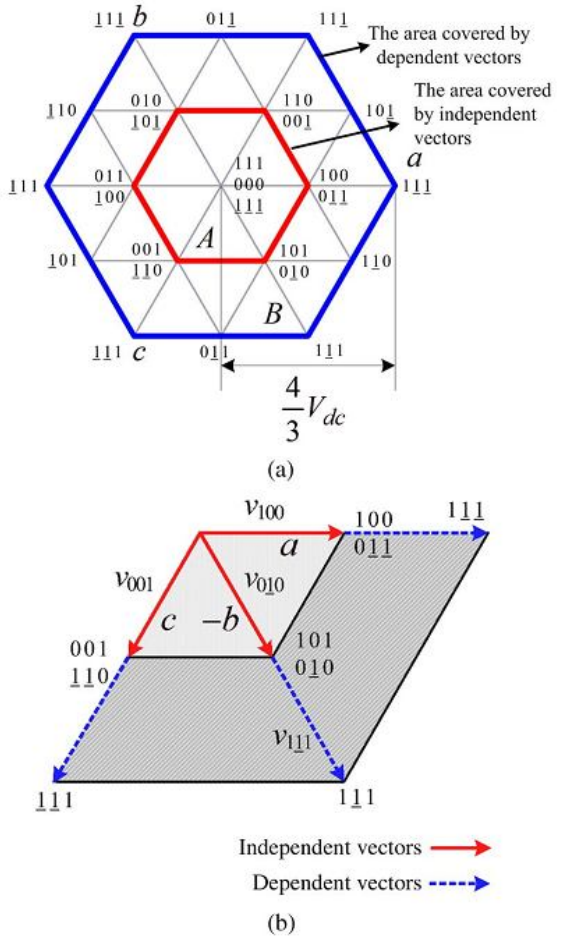

Fig. 6. Voltage vector space of one-by-three configuration MLCI.

By substituting (4) into (3), the phase voltage of each phase is represented as follows by using the relationship defined in (2):

$$v_{as} = \frac{2}{3}S_aV_{dc\_a} - \frac{1}{3}S_bV_{dc\_b} - \frac{1}{3}S_cV_{dc\_c}$$
$$v_{bs} = -\frac{1}{3}S_aV_{dc\_a} + \frac{2}{3}S_bV_{dc\_b} - \frac{1}{3}S_cV_{dc\_c}$$
$$v_{as} = -\frac{1}{3}S_aV_{dc\_a} - \frac{1}{3}S_bV_{dc\_b} + \frac{2}{3}S_cV_{dc\_c} \quad \text{----- (5)}$$

If the three dc links are balanced then V_{dc_a}, V_{dc_b}, and V_{dc_c} have the same value as magnitudes of V_{dc}, the voltage vector space in α−β coordinates is defined in Fig. 6(a) by using (5).

From the figure, it can be observed that underbars indicate the switching function has the value of −1. A part of the hexagon in Fig. 5(a) is shown in Fig. 6(b). In this figure, the vectors $v_{0\underline{1}0}$ and $v_{1\underline{1}1}$ are placed at the same reference axis, phase b. However, the constituents of those vectors are different. For $v_{0\underline{1}0}$, this vector can be synthesized without the other two phases assistance. However, $v_{1\underline{1}1}$ cannot be produced without other vectors according to (5).

From this, let the vectors which do not require other two phases assistance to be defined as "the independent vectors." Similarly, the vectors which require other phases support are defined as "the dependent vectors." According to these definitions, v_{100}, v_{001}, and $v_{0\underline{1}0}$ are the independent vectors, while$v_{1\underline{1}1}$, $v_{1\underline{1}1}$, and $v_{1\underline{1}1}$ are the dependent vectors in Fig. 6(b). Fig. 6(a) also compares the regions that can be composed by the independent

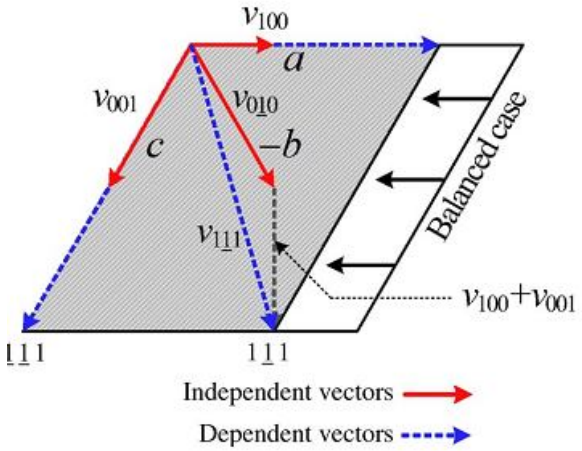

Fig. 7. Voltage vector space in an unbalanced dc-link condition.

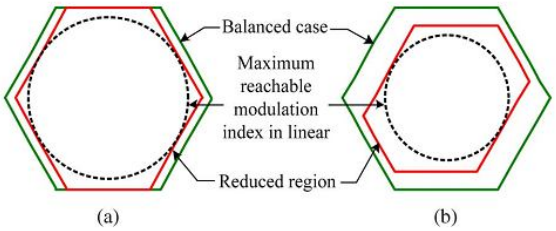

Fig. 8. Comparison of the voltage vector space under different dc-link ratios. (a) $V_{dc\_a}<V_{dc\_b}=V_{dc\_c}$. (b) $V_{dc\_b}<V_{dc\_a}<V_{dc\_c}$.

and the dependent vectors. Unlike traditional three-phase half-bridge inverters, the independent vectors can be fully applied in a switching period because the dc links in each of the three phases are separated in the given system. It should be noted that the maximum voltage is decided by the dependent vectors in the entire voltage vector space. Now, let us consider the case when a three-phase load is supplied by unequal dc links. Fig. 7 shows an extremely unbalanced case where V_{dc_a} is half of the others. If V_{dc_a} decreases, the magnitudes of the independent vectors in phase *a* are also reduced. As a result, the magnitude of v100 is decreased. Here, the phase angle of v111, which is the sum of v010, v100, and v001, is no longer matched with the angle of the independent vectors in phase *b* from the figure. As shown in the figure, if the magnitudes of the independent vectors are reduced, the available voltage vector space is also reduced, and the angles of the dependent vectors are no longer multiples of 60°. Using these properties, the voltage vector spaces in two different cases are compared in Fig. 8. In Fig. 8(a), V_{dc_a} has a lower value than the others.

In Fig. 8(b), all three dc links have different voltages. As it can be seen in Fig. 8, the original shape of the hexagon is distorted in both cases. This means that the trajectory of the maximum output voltage vector in the α–β coordinates is also distorted according to the shape of the hexagon in each. On the other hand, the magnitude of the maximum modulation index in the linear modulation range in a given hexagon corresponds to the radius of the inner circle which is inscribed in the hexagon. As shown in Fig. 8, the radius is changed as the hexagon distorts, and the achievable linear modulation range is also altered. Here, the maximum amplitude of the phase voltage V_{ph_max} in the linear modulation range is defined as

$$V_{ph\_max} = V_m\left(V_{dc\_max}\frac{\sqrt{3}}{2}\right)$$

$$V_m = \left(\frac{4}{3} - \underbrace{\frac{2}{3}\frac{V_{dc\ max} - V_{dc\ mid}}{V_{dc\_max}}}_{\substack{voltage\ limitation \\ from\ the\ medium\ dc\ link}} - \underbrace{\frac{2}{3}\frac{V_{dc\ max} - V_{dc\ min}}{V_{dc\_max}}}_{\substack{voltage\ limitation \\ from\ the\ minimum\ dc\ link}}\right) \quad \text{----(6)}$$

Where V_{dc_max}, V_{dc_mid}, and V_{dc_min} represent the maximum, medium, and minimum voltages among the dc links. In fact, (6) can be simplified as

$$V_{ph\_max} = \frac{V_{dc\_mid} + V_{dc\_min}}{\sqrt{3}} \quad \text{---- (7)}$$

It should be noted that V_{ph_max} is the maximum synthesizable voltage in the linear modulation range in the MLCI undergoing unbalanced dc-link conditions. From (7), it can be recognized that V_{ph_max} is determined by V_{dc_mid} and V_{dc_min}. If all dc links are well balanced so that V_{dc_mid} and V_{dc_min} have identical values, (7) is rewritten as

$$V_{ph\_max} = \frac{2}{\sqrt{3}}V_{dc} \quad \text{------- (8)}$$

This is exactly double the maximum synthesizable voltage in the linear modulation range of a traditional three-phase half bridge inverter. In fact, the inverter in Fig. 4 is considered as a three-phase full-bridge inverter which is fed by independent dc links. To extend the proposed approach to the multistage MLCI using PS modulation, the total dc-link voltage per phase is represented as

$$V_{dc\_P} = \sum_{j=1}^{N} V_{dc\_p(j)_{p=a,b,or\ c}} \quad \text{------ (9)}$$

Where *p* represents a certain phase among phases a, b, and c, N is the number of the power stage modules in each phase, and *j* represents the index of a power stage module in each phase. In the multistage MLCI, (9) is utilized to obtain V_{dc_max}, V_{dc_mid}, and V_{dc_min}. After that, (7) is still applied.

III. PROPOSED MODULATION TECHNIQUE

In Section II, the maximum synthesizable voltage in the linear modulation range was evaluated under the unbalanced dc links. In this section, a method is proposed to realize the maximum modulation index in the linear modulation range under these conditions.

A.CONVENTIONAL OFFSET VOLTAGE INJECTION METHOD

In this scheme an offset voltage is incorporated with phase voltage which is popularly and frequently used in three-phase half-bridge inverter applications.

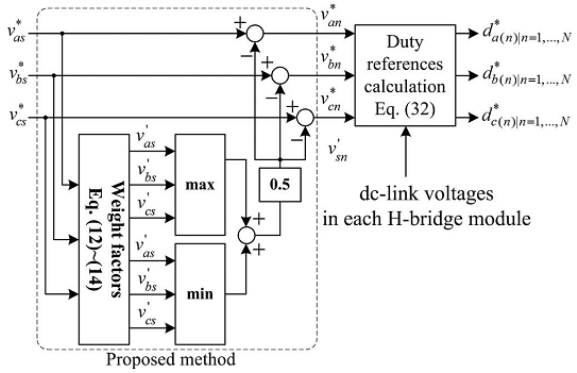

Fig. 9. Implementation of the NVM method.

To implement various PWM schemes in carrier-based PWM by using the fact those line-to-line voltages are applied to a three-phase load. The offset voltage v^*_{sn} is injected to the phase voltage references(v^*_{as},v^*_{bs},v^*_{cs}) to implement carrier-based SVPWM as in

$$v^*_{sn} = \frac{v^*_{max} + v^*_{min}}{2} \qquad v^*_{max} = \max(v^*_{as}, v^*_{bs}, v^*_{cs})$$
$$v^*_{min} = \min(v^*_{as}, v^*_{bs}, v^*_{cs}) \qquad \text{----- (10)}$$

Then, the pole voltage references v^*_{an}, v^*_{bn}, and v^*_{cn}, which will be converted to PWM duty references, are

$$v^*_{an} = v^*_{as} - v^*_{sn} \quad v^*_{bn} = v^*_{bs} - v^*_{sn} \quad v^*_{cn} = v^*_{cs} - v^*_{sn} \qquad \text{----- (11)}$$

However, the aforementioned technique may not maximize the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

B. PROPOSED NVM METHOD

If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage reference approachesV_{ph_max}. This is because the traditional methods are not considering unbalanced dc-link conditions. Therefore, even if a phase can synthesize an output voltage reference in the linear modulation range, the other phases can be saturated or go into the over modulation region. In this situation, a neutral voltage can be produced by the saturated or over modulated phase. In order to resolve this issue and to synthesize the output voltage to V_{ph_max}in the linear modulation range, the NVM technique is proposed in this paper. Fig. 8 shows the concept of the proposed NVM technique. Here, a neutral voltage between the two neutral points *n* and *s* in Fig. 4 is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant k_w is defined as

$$k_w = \frac{v^*_{dc\_mid} + v^*_{dc\_min}}{2} \qquad \text{----- (12)}$$

By using (12), the weight factors are calculated as

$$k_{w\_a} = \frac{k_w}{V_{dc\_a}} \quad k_{w\_b} = \frac{k_w}{V_{dc\_b}} \quad k_{w\_c} = \frac{k_w}{V_{dc\_c}} \qquad \text{----- (13)}$$

Wherek_{w_a}, k_{w_b}, and k_{w_c} represent the weight factors for phases a, b, and c, respectively. Next, the weight factors are multiplied by the phase voltage references, and the new referencesv'_{as}, v'_{bs}, and v'_{cs} are obtained as

$$v'_{as} = k_{w\_a} v^*_{as} \quad v'_{bs} = k_{w\_b} v^*_{bs} \quad v'_{cs} = k_{w\_c} v^*_{cs} \qquad \text{------- (14)}$$

It should be noted that, depending on dc-link conditions, the sum of v'_{as}, v'_{bs}, and v'_{cs} may not be zero. By using these components, the injected voltage v'_{sn} and the pole voltage references are given as

$$v'_{max} = \max(v'_{as}, v'_{bs}, v'_{cs}) \quad v'_{min} = \min(v'_{as}, v'_{bs}, v'_{cs})$$
$$v'_{sn} = \frac{v'_{max} + v'_{min}}{2} \qquad \begin{bmatrix} v^*_{an} \\ v^*_{bn} \\ v^*_{cn} \end{bmatrix} = \begin{bmatrix} v^*_{as} - v'_{sn} \\ v^*_{bs} - v'_{sn} \\ v^*_{cs} - v'_{sn} \end{bmatrix} \qquad \text{-----(15)}$$

From (15), the line-to-line voltages across each phase of the load are represented as

$$\begin{bmatrix} v^*_{ab} \\ v^*_{bc} \\ v^*_{ca} \end{bmatrix} = \begin{bmatrix} v^*_{an} - v^*_{bn} \\ v^*_{bn} - v^*_{cn} \\ v^*_{cn} - v^*_{an} \end{bmatrix} == \begin{bmatrix} v^*_{as} - v'_{sn} - v^*_{bs} + v'_{sn} \\ v^*_{bs} - v'_{sn} - v^*_{cs} + v'_{sn} \\ v^*_{cs} - v'_{sn} - v^*_{as} + v'_{sn} \end{bmatrix} = \begin{bmatrix} v^*_{as} - v^*_{bs} \\ v^*_{bs} - v^*_{cs} \\ v^*_{cs} - v^*_{as} \end{bmatrix} \qquad \text{-----(16)}$$

As it can be seen in (16), v'_{sn} does not appear in the line-to-line voltages, and it is still considered as a hidden freedom of voltage modulation. Now, let us consider the role of the weight factors k_{w_a}, k_{w_b}, and k_{w_c}, which are inversely proportional to the

corresponding dc-link voltage. For convenience, let us assume that the magnitudes of the dc-link voltage are under the following relationship:

$$V_{dc\_a} < V_{dc\_b} < V_{dc\_c} \quad \text{--- (17)}$$

Then, from (13) and (17)

$$k_{w\_a} > k_{w\_b} > k_{w\_c} \quad k_{w\_a} > 1 \quad k_{w\_b}, k_{w\_c} < 1 \quad \text{----- (18)}$$

Equation (18) gives

$$|v'_{as}| > |v^*_{as}| \quad |v'_{bs}| < |v^*_{bs}| \quad |v'_{cs}| < |v^*_{cs}| \quad \text{----- (19)}$$

From (15) and (19), it can be recognized that, v'_{as}, whose dc-link voltage is less than the others, is corresponding to V'_{max} orV'_{min} , the absolute value of v'_{sn} is greater than v^*_{sn} in (10). On the other hand, the final pole voltage referencesV^*_{sn}, V^*_{bn}, and V^*_{cn} are calculated by subtracting v'_{sn} from the original phase voltage referencesv^*_{as}, v^*_{bs}, and v^*_{cs} as in (15). From this reasoning, in this example, it is supposed that, if v'_{as} is corresponding to v'_{max}, then the final pole voltage references v^*_{an}, v^*_{bn}, and v^*_{cn} are less than the original pole voltage references

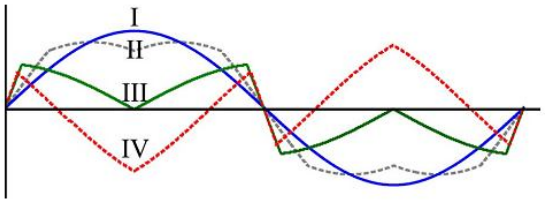

Fig. 10. Comparison of modulated waveforms. (i) Without V^*_{sn} . (ii) Traditional carrier-based SVPWM. (iii) Proposed NVM with V_{dc_a}=0.275V_{dc}, V_{dc_b} =V_{dc}, and V_{dc_c}=V_{dc}. (iv)Proposed NVM with V_{dc_a}=0.2V_{dc}, V_{dc_b} =V_{dc}, and V_{dc_c}=V_{dc}.

Which are not V'_{sn} but V^*_{sn}. On the contrary, if V'_{cs} isV'_{max}, then the final pole voltage references are greater than the original pole voltage references. By using this principle, the proposed method reduces the portion of the phase whose dc-link voltage is smaller than the others and increases the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, as it can be seen in (16), v'_{sn} does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one derived from the original phase voltage reference. From this analysis, the proposed method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. In addition to this, if all of the dc-link voltages are well balanced so thatV_{dc_a}, V_{dc_b}, and $V_{dc_c}$are equal to V_{dc}

$$V_{dc\_mid} = V_{dc\_min} = V_{dc} \quad \text{---- (20)}$$

By substituting (20) into (12)–(14)

$$k_w = \frac{V_{dc\_mid} + V_{dc\_min}}{2} = V_{dc}$$
$$k_{w\_a} = k_{w\_b} = k_{w\_c} = 1$$
$$v'_{as} = v^*_{as} \quad v'_{bs} = v^*_{bs} \quad v'_{cs} = v^*_{cs} \quad \text{---- (21)}$$

Equation (21) shows that the proposed method gives the same voltage references as the traditional method under balanced dc-link conditions.

C. CONSTRAINTS OF THE PROPOSED METHOD

In this section, the limitation of how unbalanced dc links can be while still being compensated by the proposed method is evaluated. Fig. 10 shows the modulated voltage waveforms with different modulation methods and dc-link conditions. In the figure, cases I and II show the results of traditional sinusoidal PWM (SPWM) and carrier-based SVPWM, while cases III and IV illustrate the waveforms of the proposed method with different ratios of dc-link voltages. The fundamental idea to examine the limitation of the proposed method is to evaluate what conditions bring the different polarities between the original voltage reference and the modified voltage reference by using the proposed method. In Fig. 10, the vertices at π/2 and 3π/2rad almost come in contact with, but do not cross, the zero point. However, the directions of the vertices are opposite the original phase voltage reference in case IV. This means that an excessive and unnecessary voltage is injected into the system. As a result,

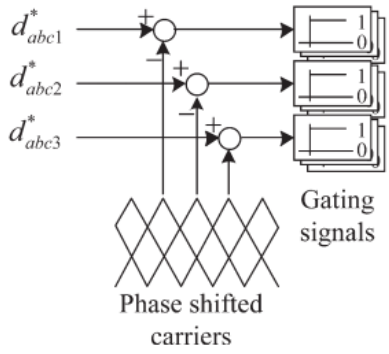

Fig. 11. Comparison of the duty references and the carriers.

INTERNATIONAL JOURNAL OF RESEARCH
In Advanced Engineering Technologies

Volume 4, Issue 5 AUG 2015

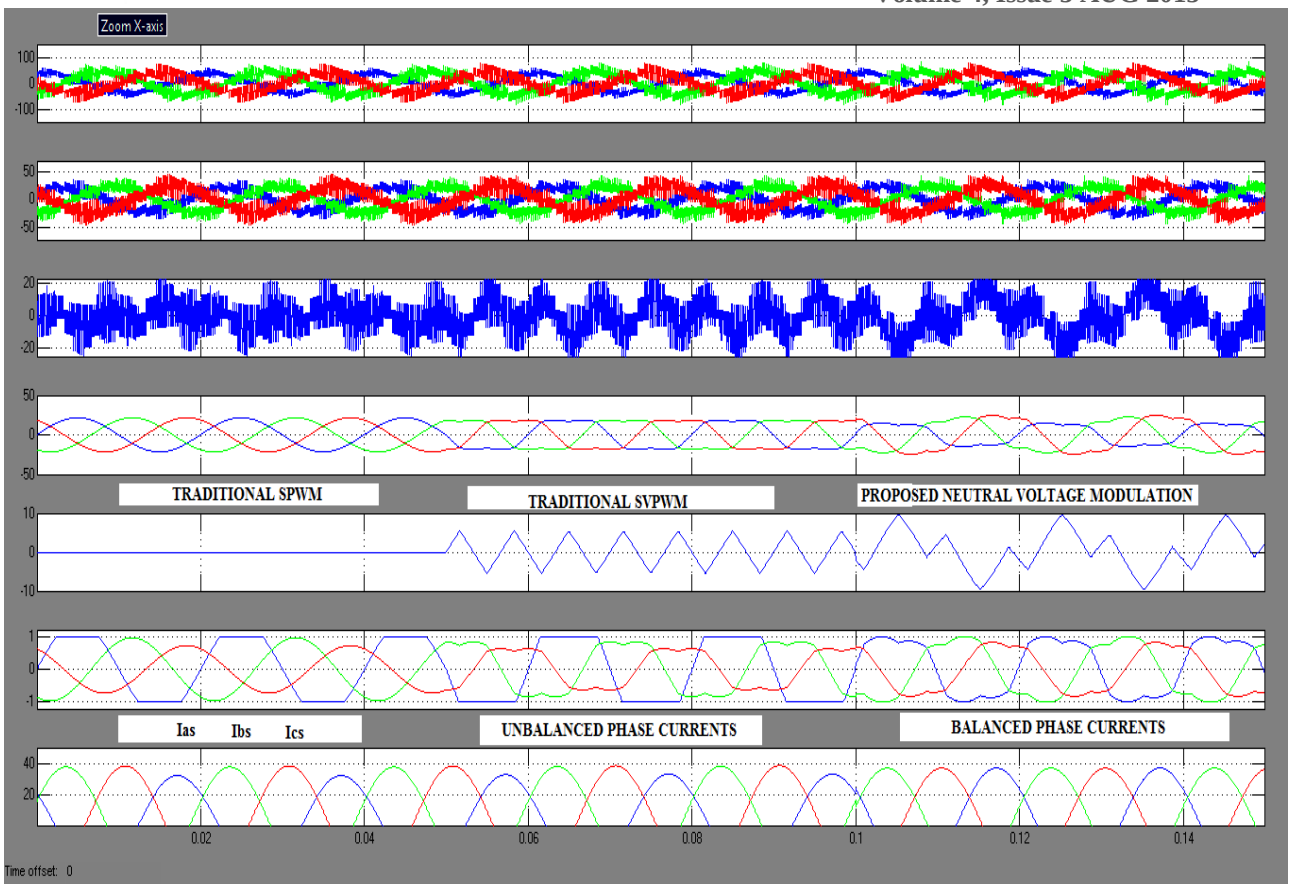

Fig. 13. Simulation result of traditional SPWM, Traditional SVPWM and the proposed method.

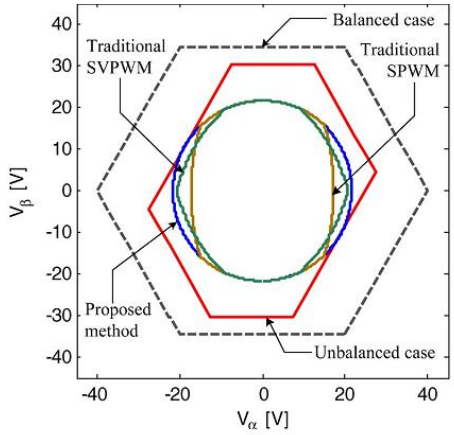

Fig. 12. Comparison of the voltage vector trajectories.

The maximum linear modulation range is reduced, and the line-to-line voltage may be distorted. With this basic concept, it is assumed that a phase which has the lowest dc-link voltage commands $V_{\max}^{*}$ and a phase which has the highest dc-link voltage commands V_{m}^{*} into examine a worst case situation.

From (14) and (15), the following equations can be established:

$$v'_{max} = \frac{V_{dc\_min} + V_{dc\_min}}{2V_{dc\_min}} v^{*}_{max}$$

$$v'_{min} = \frac{V_{dc\_mid} + V_{dc\_min}}{2V_{dc\_max}} v^{*}_{min}$$

$$v'_{max} = \frac{v'_{max} + v'_{min}}{2}$$

------ (22)

By using (22), the pole voltage reference which is considered as the worst case is

$$v^{*}_{\max\_n} = v^{*}_{max} - \frac{v'_{max} + v'_{min}}{2}$$

------ (23)

By substituting (22) into (23), we have

$$v^*_{\max\_n} = \left(1 - \frac{V_{dc\_mid} + V_{dc\_min}}{4V_{dc\_min}}\right) v^*_{max}$$
-------- (24)

Unless all three-phase voltage references are not zero simultaneously, near a positive peak of the original voltage reference, the sufficient condition which guarantees the same polarity between v^*_{max} and v^*_{min} is established as follows:

$$v^*_{\max\_n} > 0 \quad v^*_{\max} > 0 \quad v^*_{\min} < 0$$
------ (25)

By substituting (24) into the first condition in (25), the following condition can be written:

$$k_1 v^*_{max} > k_2 v^*_{min} \qquad k_1 = 1 - \frac{V_{dc\_mid} + V_{dc\_min}}{4V_{dc\_min}}$$
$$k_2 = \frac{V_{dc\_mid} + V_{dc\_min}}{4V_{dc\_max}}$$
--------- (26)

Here, it is obvious that k_2 is always positive. Therefore, as long as $k_1$is positive, the condition (26) is always satisfied, and k_1 can be rearranged as follows:

$$k_1 = \left(1 - \frac{V_{dc\_mid} + V_{dc\_min}}{4V_{dc\_min}}\right)$$
------ (27)

Equation (28) is then directly obtained from (27) to ensure that $k_1$will always be positive

$$V_{dc\_min} > \frac{1}{3} V_{dc\_mid}$$
-------- (28)

$$v^*_{\max\_n} = -2v^*_{min}$$
------ (29)

$$-2k_1 > k_2$$
---- (30)

Since k_1 is negative in this case, the following condition is derived from (30);

$$|k_1| < \frac{k_2}{2}$$
------ (31)

If the relationship betweenk1andk2is established as in (31), even if the provision in (28) is broken, the conditions in (25) are satisfied so that the proposed method can be still effective. Let us recall Fig. 10 again here. In the figure, the values of |k1| andk2/2for case III are evaluated as 0.1591 and 0.1593, respectively. Although the difference between the two values is very small, (31) is still true with these values. For case IV, the values of $|k_1|$ and $\frac{k_2}{2}$ are calculated as 0.5 and 0.3, respectively. In contrast to case III, (31) is no longer satisfied, and the directions of the vertices are opposite, as explained previously. From the analysis in this section, both the methods in (28) and (31) are successfully able to judge the availability of the proposed method. In terms of accuracy, the latter may give better results. However, in practice, the former may be useful to judge the operation of the proposed method because it is already dealing with an extremely worst case on its own and the calculation in real time is much simpler than (31).

D. DUTY CALCULATION

In Fig. 9, the final voltage references are entered to the duty reference calculation block. In this block, the duty references of each H-bridge module are calculated as follows:

$$d^*_{a1} = d^*_{a1} = \cdots = d^*_{aN} = \frac{v^*_{an}}{V_{dc\_a}}$$
$$d^*_{b1} = d^*_{b1} = \cdots = d^*_{bN} = \frac{v^*_{bn}}{V_{dc\_b}}$$
$$d^*_{c1} = d^*_{c1} = \cdots = d^*_{cN} = \frac{v^*_{cn}}{V_{dc\_c}}$$
----- (32)

The calculated duty references are compared to PS carriers to generate gating signals, as shown in Fig. 11. It should be noted that the duty references for each H-bridge in each phase are shared in the PS modulation.

IV. SIMULATION

A simple one-by-three configuration MLCI model is built in Matlab Simulink. The three-phase RLload with R=0.1Ωand L=1mH is employed. The dc-link voltages for each phase are Vdc_a=0.5×30V, Vdc_b=0.75×30V, and Vdc_c=30V. From (7), the maximum synthesizable phase voltage in linear is Fig. 12. Simulation results showing references (*Vab*, *Vbc* and *Vca*), output phase voltages (*Vxn* , *Vyn* , and *Vzn*) and output line current (*Ix* , *Iy* , and *Iz*) waveforms if “bridge—b” fails at front-end supplying output power 12.5% of rated load. zero provided components design and selection (ratings) is done to withstand it. If the HF transformers could be designed with a very low leakage inductance (negligible or significantly less of the order of nH

or<1μH), then even a single cell would be able to support rated load or nearly rated load.

$$V_{ph\_max} = \frac{0.75 \times 30 + 0.5 \times 30}{\sqrt{3}} = 21.65\ \text{V}. \quad \text{------ (33)}$$

The voltage references are given by

$$\begin{aligned} v_{as}^{*} &= V_{\text{ph\_max}} \sin(100\pi t) \\ v_{bs}^{*} &= V_{\text{ph\_max}} \sin(100\pi t - 2\pi/3) \\ v_{cs}^{*} &= V_{\text{ph\_max}} \sin(100\pi t + 2\pi/3) \end{aligned} \quad \text{------ (34)}$$

Equation (34) is applied to the modulators of the inverter in open loop. Fig. 12 compares the voltage vector spaces and the voltage trajectories in the α–β-axes of traditional SPWM, traditional SVPWM, and the proposed NVM method under the given simulation condition. Compared to the balanced dc-link case, the area of the voltage vector space is reduced under the unbalanced dc-link condition. In the figure, the traditional SPWM shows the worst voltage distortion and the minimum voltage vector space.

The traditional SVPWM gives more area than SPWM, but still, the voltage distortion is not avoidable. The proposed method shows no distortion on the output voltage and maximizes the voltage vector space compared to other methods. Fig. 13 shows the time-domain simulation results with the same simulation condition. From t=0.0s tot= 0.05s, traditional SPWM is used. From t=0.05s tot=0.1s, traditional SVPWM is used. After t=0.1 s, the proposed method is applied.

When traditional SPWM is applied, v_{sn}^{*} is zero, and the pole voltage references are identical to the ones in (34). With traditional SVPWM v_{sn}^{*} is no longer zero, and the peak voltage of the pole voltage references is reduced compared to SPWM. However, the duty reference of phase a, where the dc-link voltage is minimum among the three phases, is saturated in both cases. Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in v_{sn}^{*}, and the duty references are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current in the last section of the figure. Under traditional methods, the phase currents are unbalanced. However, the phase currents are well balanced with the proposed method. From the simulation results, it can be seen that the proposed method can synthesize the maximum available phase voltage in the linear modulation range under unbalanced dc link.

V. CONCLUSION

In this paper 7-level MLCI has been enforced with Neutral Voltage Modulation technique for underneath balanced DC-link conditions. so as to research the most synthesizable voltage of MLCIs, the voltage vector house has been analyzed exploitation the switch perform. From the analysis, the limit is meant for linear modulation. NVM is employed to get most modulation index in linear modulation vary underneath associate unbalanced dc-link condition still on balance the output part voltages. compared to previous ways the planned methodology is definitely enforced and output voltage quality underneath unbalanced dc-link conditions. Simulations results supported the IPM motor drive application is verified for the effectiveness of the planned methodology.

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