INTERNATIONAL JOURNAL OF RESEARCH
In Advanced Engineering Technologies

Volume 4, Issue 5 AUG 2015

A New Switching Algorithm for Reduced Number of Power Electronic Components Multilevel Inverter

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Abstract— during this paper, a replacement configuration of a three-phase nine-level construction voltage-source converter is introduced. A construction dc link mistreatment mounted dc voltage provides and cascaded half-bridge is connected in such however that the projected converter outputs the required output voltage levels. the fundamental frequency steps modulation technique is certainly used to generate the acceptable modification gate signals. For the aim of fast range|the amount the quantity of voltage levels with fewer variety of power electronic elements, the structure of the projected converter is extended and utterly alternative ways to figure out the magnitudes of used dc voltage provides unit of measurement suggested. Moreover, the paradigm of the suggested configuration is factory-made as a result of the obtained simulation and hardware results ensured the practicableness of the configuration and thus the compatibility of the modulation technique is accurately noted. of the modulation technique is accurately noted.

***Index Terms*—Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter.**

I.INTRODUCTION

Multilevel inverters accommodates a bunch of switch devices and dc voltage provides, the output of that produces voltages with stepped waveforms. construction technology has started with the three-level device followed by various construction device topologies. completely different topologies and wide range of management strategies are developed within the recentliterature [1]–[3]. the foremost common construction electrical converter configurations area unit neutral purpose clamped (NPC), the flying condenser (FC), and therefore the cascaded H-bridge (CHB). The deviating voltage of neutral-point voltage in agency, the unbalanced voltage within the dc link of FC, and therefore the sizable amount of separated dc provides in CHB area unit thought of the most drawbacks of those topologies [4], [5]. except for these 3 main topologies, alternative topologies area unit introduced [6]–[17].

Recently, asymmetrical and hybrid period of time topologies are getting one in all the foremost interested analysis space. within the asymmetrical configurations, the Magnitudes of dc voltage provides area unit unequal. These topologies scale back the value and size of the electrical converter and improve the dependableness since minimum variety of power electronic parts, capacitors, and dc provides area unit used. The hybrid period of time converters accommodates completely different construction configurations with unequal dc voltage provides. With such converters, completely different modulation ways and power electronic parts technologies area unit required [18]–[26]. On the opposite hand, for the aim of up the performance of the traditional single- and three-phase inverters, completely different topologies using differing kinds of duplex switches are prompt in [27]–[29].

Scrutiny to the simplex one, duplex switch is ready to conduct this and withstanding the voltage in each directions. duplex switches with AN applicable management technique will improve the performance of construction inverters in terms of reducing the amount of semiconductor parts, minimizing the withstanding voltage and achieving the required output voltage with higher levels [30]–[34]. supported this technical background, this paper suggests a unique topology for a 3 part nine-level construction electrical converter. the amount of switch devices, insulated-gate driver circuits, and installation space and value area unit considerably reduced. The magnitudes of the used dc voltage provides are elect in an exceedingly approach that brings the high variety of voltage level with a good application of a harmonic way modulation technique. Extended structure for N-level is additionally

bestowed and compared with the traditional well-known construction inverters. Simulation and hardware results area unit given and explained.

II. Proposed Topology

Fig. 1 shows the typical configuration of the proposed three-phase nine-level multilevel inverter. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level

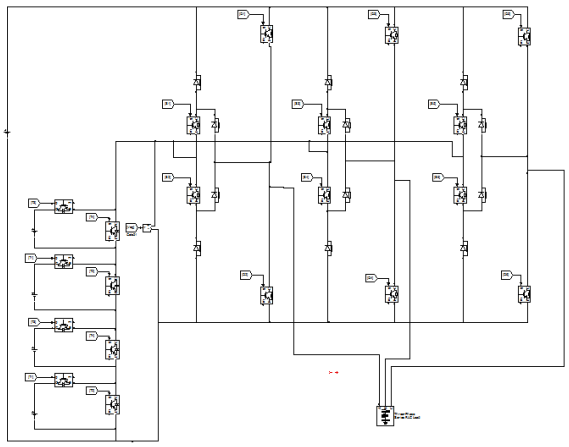

Fig. 1. Circuit diagram of the proposed three-phase 9-level multilevel inverter

bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of $4V_{dc}$ and CHB having four dc voltage supplies of V_{dc}, V_{dc} and $2V_{dc}$, $2V_{dc}$ are connected to (+, –, o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve nine voltage levels, the power circuit of the CHB makes use of four series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output different voltage levels. The first cell dc voltage supply V_{dc} is added if switch T1 is turned ON leading to $V_{mg} = +V_{dc}$ where V_{mg} is the voltage at node (*m*) with respect to inverter ground (*g*) or bypassed if switch T2 is turned ON leading to $V_{mg} = 0$. Likewise, the second cell dc voltage supply $2V_{dc}$ is added when switch T3 is turned ON resulting in $V_{om} = +2V_{dc}$ where V_{om} is the voltage at midpoint (*o*) with respect to node (*m*) or bypassed when switch T4 is turned ON resulting in $V_{om} = 0$. The peak voltage rating of the switches of the conventional two level bridge (Q1–Q6) is $4V_{dc}$ whereas the bidirectional switches (S1–S6) have a peak voltage rating of $3V_{dc}$. In CHB cells, the peak voltage rating of second cell switches (T3 and T4) is $2V_{dc}$ while the peak voltage rating of T1 and T2 in the first cell is V_{dc}. By considering phase *a*, the operating status of the switches and the inverter line-to-ground voltage V_{ag} are given in Table I.

TABLE I
Switching State *Sa* and Inverter Line-to-Ground Voltage V_{ag}

S_a	Q1	S1	S2	Q2	T1	T2	T3	T4	V_{ag}
4	on	off	off	off	on	off	on	off	$+4V_{dc}$
3	off	On	on	off	on	off	on	off	$+3V_{dc}$
2	off	On	on	off	off	on	on	off	$+V_{dc}$
1	off	On	on	off	on	off	off	on	$+V_{dc}$
0	off	off	off	On	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages V_{ag}, V_{bg}, and V_{cg} in terms of switching states *Sa*, *Sb*, and *Sc* as

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \qquad (1)$$

where $N = 5$ is the maximum number of voltage levels. The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The inverter may have 24 different modes within a cycle of the output waveform. According to Table II, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state. As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current I_b can flow in S3 and Db1 or S4 and Db2). Since some insulated gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms V_{ab}, V_{bc}, and V_{ca} with corresponding switching gate signals are depicted in Fig. 2 where V_{ab}, V_{bc}, and V_{ca} are related to V_{ag}, V_{bg}, and V_{cg} by

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \qquad (2)$$

The inverter line-to-neutral voltages V_{aN}, V_{bN}, and V_{cN} may be expressed as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (3)$$

It is useful to recognize that the inverter voltages at terminals *a*, *b*, and *c* with respect to the midpoint (*o*) are given by

$$\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} - \begin{bmatrix} V_{og} \\ V_{og} \\ V_{og} \end{bmatrix} \quad (4)$$

where V_{og} is the voltage at midpoint (*o*) with respect to ground (*g*). V_{og} routinely fluctuates among three different voltage values V_{dc}, $2V_{dc}$, and $3V_{dc}$ as follows: $+8V_{dc}/3$, $+7V_{dc}/3$, $+6V_{dc}/3$, $+5V_{dc}/3$, $+4V_{dc}/3$, $+2V_{dc}/3$, 0, $-2V_{dc}/3$, $-4V_{dc}/3$, $-5V_{dc}/3$, $-6V_{dc}/3$, $-7V_{dc}/3$, and $-8V_{dc}/3$.

It is worth noting that all simulated waveforms are obtained at $t_1 = t_2 = \cdots = t_{24} = 0.02/24$ s.

$$V_{og} = \begin{cases} V_{dc}, & if\ S_a + S_b + S_c \leq 5 \\ 2V_{dc}, & if\ S_a + S_b + S_c = 6 \\ 3V_{dc}, & if\ S_a + S_b + S_c \geq 7 \end{cases} \quad (5)$$

The simulated voltage waveforms of V_{ag}, V_{og}, V_{ao} and V_{aN} based on (1)–(5) are shown in Fig. 3 where, for instance, 13 sequent voltage steps are seen in V_{aN} waveform as follows:

TABLE II
SWITCHING STATES SEQUENCE OF THE PROPOSED INVERTER WITHIN ONE CYCLE

$S_a S_b S_c$	Period T[s]	ON switches Leg a	ON switches Leg b	ON switches Leg c	ON switches Cascaded half-bridge	V_{ag}	V_{bg}	V_{cg}
400	t1	Q1	Q4	Q6	T1, T4	$4V_{dc}$	0	0
410	t2	Q1	S3, S4	Q6	T1, T4	$4V_{dc}$	V_{dc}	0
420	t3	Q1	S3, S4	Q6	T2, T3	$4V_{dc}$	$2V_{dc}$	0
430	t4	Q1	S3, S4	Q6	T1, T3	$4V_{dc}$	$3V_{dc}$	0
440	t5	Q1	Q3	Q6	T1, T3	$4V_{dc}$	$4V_{dc}$	0
340	t6	S1,S2	Q3	Q6	T1, T3	$3V_{dc}$	$4V_{dc}$	0
240	t7	S1,S2	Q3	Q6	T2, T3	$2V_{dc}$	$4V_{dc}$	0
140	t8	S1,S2	Q3	Q6	T1, T4	V_{dc}	$4V_{dc}$	0
040	t9	Q2	Q3	Q6	T1, T4	0	$4V_{dc}$	0
041	t10	Q2	Q3	S5, S6	T1, T4	0	$4V_{dc}$	0
042	t11	Q2	Q3	S5, S6	T2, T3	0	$4V_{dc}$	V_{dc}
043	t12	Q2	Q3	S5, S6	T1, T3	0	$4V_{dc}$	$2V_{dc}$
044	t13	Q2	Q3	Q5	T1, T3	0	$4V_{dc}$	$3V_{dc}$
034	t14	Q2	S3, S4	Q5	T1, T3	0	$3V_{dc}$	$4V_{dc}$
024	t15	Q2	S3, S4	Q5	T2, T3	0	$2V_{dc}$	$4V_{dc}$
014	t16	Q2	S3, S4	Q5	T1, T4	0	V_{dc}	$4V_{dc}$
004	t17	Q2	Q4	Q5	T1, T4	0	0	$4V_{dc}$
104	t18	S1,S2	Q4	Q5	T1, T4	V_{dc}	0	$4V_{dc}$
204	t19	S1,S2	Q4	Q5	T2, T3	$2V_{dc}$	0	$4V_{dc}$
304	t20	S1,S2	Q4	Q5	T1, T3	$3V_{dc}$	0	$4V_{dc}$
404	t21	Q1	Q4	Q5	T1, T3	$4V_{dc}$	0	$4V_{dc}$
403	t22	Q1	Q4	S5, S6	T1, T3	$4V_{dc}$	0	$3V_{dc}$
402	t23	Q1	Q4	S5, S6	T2, T3	$4V_{dc}$	0	$2V_{dc}$
401	t24	Q1	Q4	S5, S6	T1, T4	$4V_{dc}$	0	V_{dc}

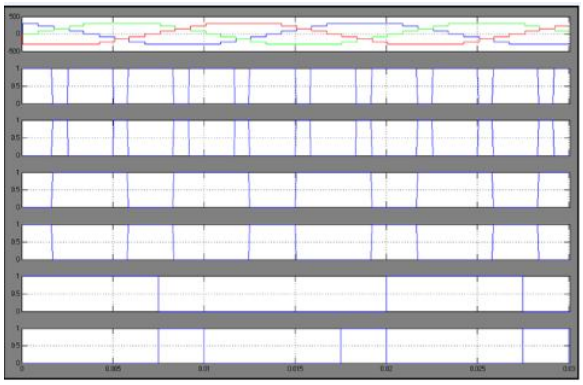

Fig. 2. Simulated waveforms of V_{ab} , V_{bc} , and V_{ca} with corresponding switching gate signals for the proposed inverter at fundamental frequency f = 50 Hz.

In order to plot the space vector diagram of the proposed inverter in a stationary *d–q* reference frame, the following equations can be used to derive *d* and *q* voltage components for all inverter vectors:

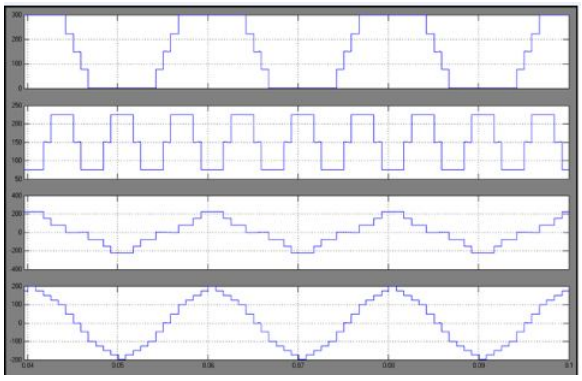

Fig. 3. Simulated waveforms of V_{ag}, V_{og}, V_{ao} and V_{aN} for the proposed inverter f = 50 Hz.

$$V_q = \frac{4V_{dc}}{3(N-1)}(2S_a - S_b - S_c) \qquad (6)$$

$$V_d = \frac{4V_{dc}}{\sqrt{3}(N-1)}(S_c - S_b) \qquad (7)$$

$$V = V_q - jV_d \qquad (8)$$

For all switching states presented in Table II, Fig. 4 shows the space vector diagram for the proposed topology.

III. Switching Algorithm

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms. An iterative method such as the Newton–Raphson method is normally used to find the solutions to (*N*–1) nonlinear transcendental equations. The difficult calculations and the need of high performance controller for the real application are the main disadvantages of such method. Therefore, an alternative method is proposed to generate the inverter's switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of *Sa*, *Sb*, and *Sc*. The basis of the proposed method can be explained as following: For a given value of modulation index M_a and within a full cycle of

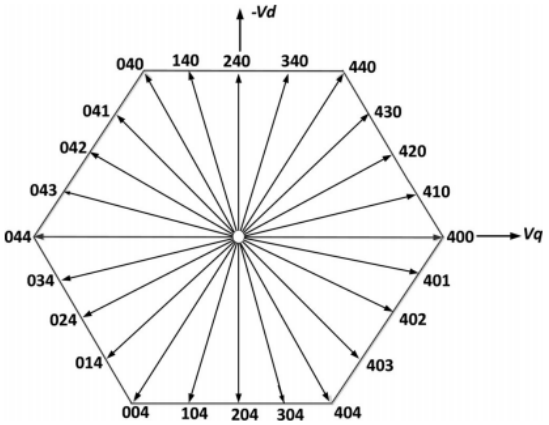

Fig. 4. Switching states vectors of the proposed inverter in *d–q* reference frame.

the operation of the proposed inverter, the switching states *Sa*, *Sb*, and *Sc* are determined instantaneously. The on-time calculations of *Sa*, *Sb*, and *Sc* directly depend on the instantaneous values of the inverter line-to-ground voltages. It is well known that the reference values of V_{ag}, V_{bg}, and V_{cg} are normally given by

$$\begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} + \frac{4V_{dc}}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \qquad (9)$$

where *wt* is the electrical angle. Or

$$\begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} + \frac{4V_{dc}}{2} * \left[1 - \frac{M_a}{6}\cos(3\omega t)\right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (10)$$

From (10), it can be noticed that the third harmonic component is added to the three-line-to-ground voltages. The third harmonic injection may increase the inverter fundamental voltage without causing over modulation. As a result, M_a can reach to 1.15 and *Sa*, *Sb*, and *Sc* can be simply determined by integering the reference line-to-ground voltages as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = integer \left(\frac{N-1}{4V_{dc}} * \begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} \right) \quad (11)$$

Comparison of the proposed modulation method with the staircase modulation with the selective harmonic method shows that the proposed modulation features less time and needs simple calculations. The inverter's operating switching states *Sa*, *Sb*, and *Sc* and corresponding switching gate signals based on the proposed modulation method are shown in Fig. 5. It is clear

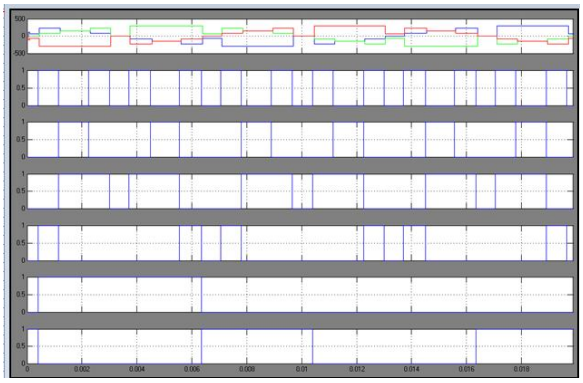

Fig. 5. Inverter's operating switching states *Sa*, *Sb*, and *Sc* with corresponding switching gate signals based on the proposed modulation method.

TABLE III
SWITCHING STATE Sa1 AND INVERTER LINE-TO-GROUND VOLTAGE V_{ag}

AT $M_a < 0.9$ (LEG *a*)

Sa1	Q1	S1	S2	Q2	T1	T2	T3	T4	V_{ag}
2	On	Off	Off	Off	Off	On	On	Off	+4Vdc
1	Off	On	On	Off	Off	On	On	Off	+2Vdc
0	off	Off	off	on	Off	On	On	Off	0

that the switching gate signals are generated within 24 different modes starting from (044) to (034). Since the proposed inverter has been designed to achieve nine voltage levels, the modulation index must be within range $0.9 \leq M_a \leq 1.15$. For modulation index $M_a < 0.9$, only two dc voltage supplies $4V_{dc}$ and $2V_{dc}$ are utilized and the behavior of the proposed inverter becomes similar to the three-level multilevel inverter. Using (9)–(11) and substituting $N = 3$, the inverter's operating switching states *Sa*, *Sb*, and *Sc* at $M_a < 0.9$ can be defined. The operation principle of the proposed inverter at $M_a < 0.9$ is illustrated in Table III. Fig. 6(a) and (b) shows the inverter line-to-line voltage waveforms at nine different modulation indices including the overmodulation operation M_a = 0.8, 0.9, 1.05, 1.15, and 1.3.

IV. EXTENDED STRUCTURE

It is noticeable that there is possibility to reach an output voltage with higher number of steps in the proposed multilevel inverter by extending the CHB circuit. Such extending can be done by adding more half-bridge cells connected in series as shown in Fig. 7(a) and (b). In order to achieve the desired number of voltage levels, three methods can be followed to determine the magnitudes of utilized dc voltage supplies.

1) All cells have an equal dc supply in magnitude.

$$V_{dc1} = V_{dc2} = \ldots = V_{dcn} = V_{dc} \quad (12)$$

Then, the magnitude of fixed dc supply can be chosen as

$$V_{fix} = (N-1)V_{dc} = (1+n)V_{dc} \quad (13)$$

where *n* is the number of utilized cells. The maximum number of voltage steps is related to the number of utilized cells by

$$N = n + 2 \quad (14)$$

The number of operation modes that makes the switching states sequence achieves the required output voltage waveform

$$M = 6(N-1) \quad (15)$$

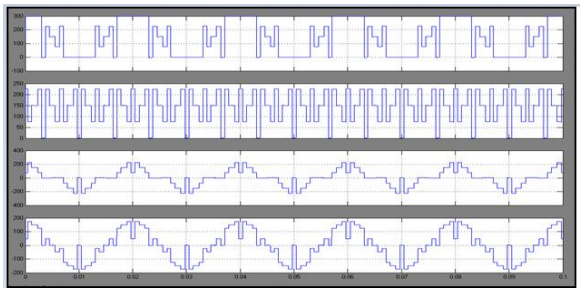

Fig. 6. Simulated waveforms of V_{ab} at different modulation indices for the proposed inverter: (a) Ma = 0.9, 1.05, and 1.15 and (b) Ma = 0.8 and 1.3. can be expressed as

2) The magnitude of dc voltage supply used in each and every cell in a particular inverter is obtained as follows:

$$V_{dc1} = V_{dc} \quad (16)$$

$$V_{dc2} = 2V_{dc} \quad (17)$$

$$V_{dcn} = nV_{dc} \quad (18)$$

$$V_{fix} = (N-1)V_{dc} = \left[1 + \frac{n(n+1)}{2}\right]V_{dc} \quad (19)$$

$$N = 2 + \frac{n(n+1)}{2} \quad (20)$$

$$M = 6(N-1) \quad (21)$$

3) By making a binary (power of 2) relationship between the dc supplies of the CHB structure as follows:

$$V_{dc1} = 2^{(0)}(V_{dc}) \quad (22)$$

$$V_{dc2} = 2^{(1)}(V_{dc}) \quad (23)$$

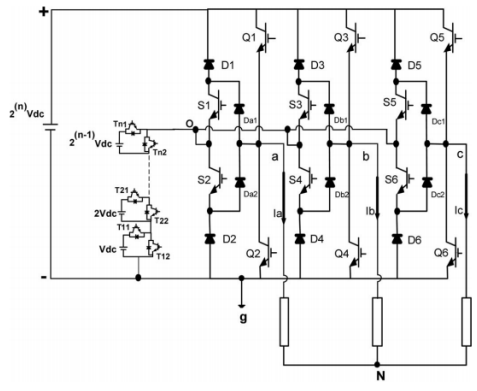

Fig. 7. Circuit diagram of the proposed three-phase N-level multilevel inverter

$$V_{dcn} = 2^{(n-1)}(V_{dc}) \quad (24)$$

$$V_{fix} = (N-1)V_{dc} = \left[1 + \sum_{j=1}^{n} 2^{j-1}\right]V_{dc} = (2^n)V_{dc} \quad (25)$$

$$N = 1 + 2^n \quad (26)$$

$$M = 6(N-1) \quad (27)$$

Table IV illustrates some characteristics of the proposed methods.

TABLE IV
COMPARISON OF THE MAXIMUM NUMBER OF VOLTAGE LEVELS WITH THE REQUIRED VALUE OF DC VOLTAGE SUPPLIES AMONG THE PROPOSED METHODS

Number of cells	1st Method			2nd Method			3rd Method		
N	N	M	V_{fix}	N	M	V_{fix}	N	M	V_{fix}
2	4	18	$3V_{dc}$	5	24	$4V_{dc}$	5	24	$4V_{dc}$
3	5	24	$4V_{dc}$	8	42	$7V_{dc}$	9	48	$8V_{dc}$
4	6	30	$5V_{dc}$	12	66	$11V_{dc}$	17	96	$16V_{dc}$
5	7	36	$6V_{dc}$	17	96	$16V_{dc}$	33	192	$32V_{dc}$
6	8	42	$7V_{dc}$	23	132	$22V_{dc}$	65	384	$64V_{dc}$

Based on the comparison carried among the proposed methods, the following are some observations. 1) Comparing to the second and third methods, the first method has a high modularity degree since the symmetric structure of CHB makes use of equal dc voltage supplies. This method helps the proposed inverter to reach all maximum number of voltage levels (4, 5, 6, 7, 8,...,*N*).

2) Since the second and third methods use the asymmetrical structure of CHB, the proposed inverter can reach the required output voltage and the maximum number of voltage levels such as 5, 8, 9, 12, 17,... with less number of dc voltage supplies and power electronic components.

V. COMPARISON STUDY

In order to investigate the capability of the suggested configuration, the proposed inverter is compared with different types of multilevel inverters such as NPC, FC, and CHB. It is evident that the suggested three-phase *N*-level multilevel inverter can considerably minimize the required number of power components. For the same number of output voltage levels ($N \geq 4$), Table V explains the required number of dc voltage supplies, switches, clamping diodes, control signals, and balancing capacitors of the proposed *N*-level inverter compared with three

existing inverters NPC, FC, and CHB. As shown in Fig. 8, it can be noticed that nearly more than two-thirds of number of switches can be counted out as N increases. For instance, at the same number of voltage levels $N = 17$, and compared with the existing multilevel inverters which require 96 switches, the required number of switches for the proposed inverter is less since it requires 42 switches based on the first method, 22 switches based on the second method, and 20 switches based on the third method. On the other hand, it is well known that the voltage and current ratings of the power components have an effect on the cost and realization of the multilevel inverter. Assuming that all power components have an equal current rating which is the rated current of the load (IL), the voltage ratings of these components depend on the magnitude of dc voltage supplies, voltage stress, and structure of the inverter. Considering that all inverters have the same input dc link which equals $(N–1)V_{dc}$, Table VI illustrates the rating requirements for the proposed inverter comparing with the rating requirements for the existing inverters. It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are involved, the semiconductor devices expenses are considerably recovered.

VI. Power Conversion Efficiency and Total Harmonic Distortion (THD%)

In order to determine the efficiency of the proposed inverter, it is necessary to determine the value of conduction and switching power losses generated by the semiconductor components. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: conduction loss (P_{con}) and switching loss (P_{sw}) as follows:

$$P_{SW\_IGBT} = \frac{1}{T}\int_0^T E_{on}(t)dt + \frac{1}{T}\int_0^T E_{off}(t)d(t) \quad (28)$$

$$P_{SW\_diode} = \frac{1}{T}\int_0^T E_{rr}(t)dt \quad (29)$$

where $E_{on}(t)$ is a turn-on loss and $E_{off}(t)$ is a turn-off loss. Switching losses $E_{on}(t)$ and $E_{off}(t)$ are experienced during the ON and OFF states, respectively. While $E_{rr}(t)$ is the reverse recovery loss of the diode, the majority of switching loss, which is experienced when the diode is turned OFF (OFF state)

$$P_{con\_IGBT} = \frac{1}{T}\int_0^T V_{on\_IGBT} i(t)dt \quad (30)$$

$$P_{con\_Diode} = \frac{1}{T}\int_0^T V_{on\_diode} i(t)dt \quad (31)$$

Conduction power losses of IGBT and diode are approximated based on their forward voltage drops $V_{on\ IGBT}$, $V_{on\ diode}$, and the instantaneous current $i(t)$ flowing through IGBT or diode. The total losses P_t are expressed as follows:

$$P_t = P_{con} + P_{sw} \quad (32)$$

Once the total semiconductors losses P_t in the introduced inverter are defined, the relative inverter efficiency is determined based on the following expression:

$$n\% = \frac{P_{out}}{P_t + P_{out}} \times 100 \quad (33)$$

Table VII provides the possible current directions with corresponding conducting devices in phase a.

MATLAB/Simulink model of the proposed inverter shown in Fig. 1 has been developed to study the conduction and switching power losses. The proposed inverter is designed to deliver output power of $P_{out} = 1.9$ kW. Three-phase series resistive–inductive (23 Ω–3 mH/Phase) in star connection is used as load. The multilevel dc link is determined as $V_{dc} = 75$ V, $2V_{dc} = 150$ V, and $V_{fix} = 4V_{dc} = 300$ V and the proposed staircase modulation technique at $M_a = 1$ is implemented to generate the appropriate switching gate signals. Three different types of semiconductor components are selected to build the prototype of the proposed inverter power circuit as following: IGBT (HGTG20N60B3D) 600 V/40 A for the two-level bridge and CHB switches, IGBT (IRG4BC40W) 600 V/20 A for bidirectional switches, and Diode (RHRP1540) 400 V/15 A for embedded diodes in

TABLE V
COMPARISON OF THE PROPOSED N-LEVEL INVERTER WITH THE EXISTING INVERTERS

Converter type	NPC	FC	CHB	Proposed		
				1st method	2nd method	3rd method
Switches	6(N-1)	6(N-1)	6(N-1)	2(N-1)+10	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Gate drivers	6(N-1)	6(N-1)	6(N-1)	2(N-1)+7	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$
Diodes	6(N-1)	6(N-1)	6(N-1)	2(N-1)+10	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Clamping diodes	6(N-2)	0	0	0	0	0
DC supplies	N-1	N-1	3(N-1)/2	N-1	$1+[(\sqrt{8N-15}-1)/2]$	$1+Log_2(N-1)$
Clamping capacitors	0	3(N-2)	0	0	0	0
Control signals	6(N-1)	6(N-1)	6(N-1)	2(N-1)+7	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$

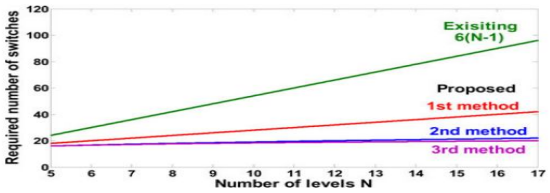

Fig. 8. Comparison of required number of switches among existing inverters and the proposed topology

bidirectional switches and freewheeling diodes. The datasheets of the utilized semiconductor components are easily accessed to acquire their characteristics curves. To simplify the losses calculation, a curve-fitting tool of MATLAB is used to approximate these curves by exponential equations [35]. The mathematical models obtained for HGTG20N60B3D 600 V/40 A are given by

$$V_{on\_IGBT1} = 1.418e^{0.016i(t)} \quad (34)$$

$$E_{on\_IGBT1} = (201.6e^{0.04418i(t)} - 291.6e^{-0.1265i(t)}) \times 10^{-6} \quad (35)$$

$$E_{off\_IGBT1} = (323.9e^{0.05125i(t)}) \times 10^{-6} \quad (36)$$

While the mathematical models obtained for IRG4BC40W 600 V/20 A are given by

$$V_{on\_IGBT2} = 1.555e^{0.0085371i(t)} \quad (37)$$

$$E_{sw\_IGBT2} = (0.3405e^{0.04472i(t)}) \times 10^{-3} \quad (38)$$

And finally, the mathematical models obtained for RHRP1540 400 V/15 A are given by

$$V_{on\_diode} = 1.325e^{0.006424i(t)} - 0.8571e^{-0.07183i(t)} \quad (39)$$

$$E_{rr\_diode} = (15.7\ e^{-0.002733i(t)} - 2.74e^{-0.1413i(t)} - 3.162\ e^{-0.05923i(t)} - 8e^{-0.09452i(t)}) \times 10^{-6} \quad (40)$$

Therefore, the conduction and switching power losses for the inverter switches and diodes can be estimated by substituting (34)–(40) into (28)–(33). e efficiency of the proposed inverter is estimated while the input voltage is raised in small steps. Fig. 9(a) depicts the estimated value of efficiency over a wide range of the output power. It is clear that the inverter's efficiency varies directly proportional to the output power and reaches its maximum value of 96.53% at 1.9 kW. It is a result of more power being effectively transferred with respect to the power losses. Furthermore, the power losses distribution among the inverter's legs and the CHB cells are shown in Fig. 9(b). The power losses distribution is obtained during the operation of the proposed inverter to deliver P_{out} = 1.287 kW at voltage step η V_{dc} = 62.5 V, $2V_{dc}$ = 125 V, and $V_{fix} = 4V_{dc}$ = 250 V. The power losses generated by legs *a*,*b*, and *c* are almost equal and slightly higher than those generated by CHB cells. According to Fig. 9(b), 53.3% of the total value of power loss is experienced in the conventional two-level bridge since 3 × 9.92 W in term of conduction power losses is generated by Q1–Q6. It is definitely due to fact that the conduction power loss is directly proportional to the switch conduction time and the value of conducting current (for instance, Q1 and Q2 conduct the load current in 18 modes). Negligible conduction power losses are generated by the free whiling diodes (D1–D6). Further measurements show that 9.68 + 2.2 W is the estimated value of the conduction power losses generated by CHB's switches and diodes. It is almost 21.3% of total power loss. The higher conduction power loss is experienced in T3 followed by T1, T4, and T2. The three bidirectional switches contribute to 19.6% of the total power loss as 3 × 3.66 W is the estimated value of conduction power loss generated by S1–S6 and Da1–Dc2. Finally, it can be observed that a negligible switching loss is generated since the fundamental frequency is implemented.

TABLE VI
PROPOSED AND THE EXISTING TOPOLOGIES RATING REQUIREMENTS PER LEVEL *N*

Proposed inverter	Main bridge Q1~Q6 D1a-D2c	Bidirectional Switches S1 to S6 D1 to D6	Cascaded half bridge switches T11 to Tn2			Converter type	NPC	FC	CHB
			1st method	2nd method	3rd method	Switches voltage rating	Vdc	Vdc	Vdc
Component voltage rating	(N-1)Vdc	(N-2)Vdc	Vdc	nVdc	$2^{(n-1)}$Vdc	Clamping Diode voltage rating	Vdc	0	0
						Clamping capacitor voltage rating	0	Vdc	0
Active component current	IL	IL	IL	IL	IL	Active component current	IL	IL	IL

TABLE VII
CONDUCTING DEVICES OF THE PROPOSED INVERTER PHASE *a*

Current	Conducting Devices Phase a. Fig.1(a)	Vag	Conducting Devices Phase a. Fig.1(a)	Vag
Ia>0	Q1	+4Vdc	Q1	+4Vdc
	T1, T3, S2, Da2	+3Vdc	T1, T3, S2, Da2	+3Vdc
	Dz2, T3, S2, Da2	+2Vdc	Dz2, T3, S2, Da2	+2Vdc
	T1, Dz4, S2, Da2	+Vdc	T1, Dz4, S2, Da2	+Vdc
	D2, Da2	0	D2	0
Ia<0	D1, Da1	+4Vdc	D1	+4Vdc
	Dz1, Dz3, S1, Da1	+3Vdc	Dz1, Dz3, S1, Da1	+3Vdc
	T2, Dz3, S1, Da1	+2Vdc	T2, Dz3, S1, Da1	+2Vdc
	Dz1, T4, S1, Da1	+Vdc	Dz1, T4, S1, Da1	+Vdc
	Q2	0	Q2	0

The estimated value of efficiency and power losses distribution of the NPC multilevel inverter are shown in Fig. 9(c) and (d). Comparison of the proposed inverter' efficiency with the nine-level NPC multilevel inverter's efficiency shows that the proposed inverter has a higher efficiency since the maximum estimated efficiency of the NPC multilevel inverter
is 93.85%. The lower P_t generated by the proposed inverter comparing with P_t generated by the nine-level NPC multilevel inverter is a result of the low conduction power losses and reduced number of power components. A lower voltage stress leads to a lower switching power loss. However, the more the switching devices, the higher the conduction power losses. At the same operating point $P_{out} \approx 1.287$ kW and compared with the estimated value of $P_{t\ proposed} = 3 \times 14.4 + 12.78 \approx 55.9$ W generated by the proposed inverter, the estimated value of P_t

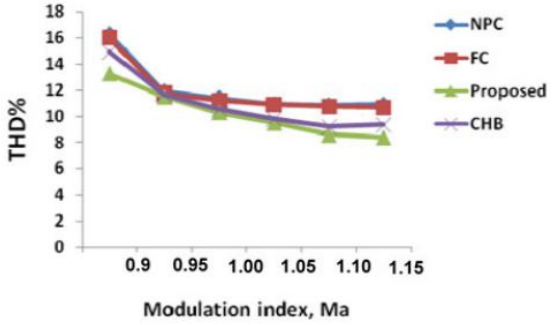

Fig. 10. NPC, FC, CHB, and proposed inverter: line-to-line voltage THD% versus M_a .

generated by the NPC multilevel inverter is two times higher. It is nearly $P_{t\ NPC} = 3 \times 37.5 \approx 112.5$ W. Moreover, the proposed inverter has been tested under different modulation indices (M_a = 0.9, 1, and 1.15). THD% of the output voltage can be calculated by

$$\text{THD\%} = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} \times 100\% \qquad (41)$$

where V_1 and V_k are the fundamental component and harmonic order, respectively. NPC, FC, and CHB multilevel inverters have been tested under the same

operating conditions. The goal of this test is to compare the proposed inverter with the existing inverters in term of THD%. Fig. 10 depicts THD% of the line to line voltage for all inverters within specific range of modulation indices [0.9–1.15]. It can be seen that the THD% of all inverter is slightly different. The measured values of THD% for the proposed inverter are within a range of 8.4–13.25%. As a result, the proposed inverter essentially adds the attractive aspects of the traditional two-level inverter such as less power components, simple working principle, and minimum conduction power loss to the main advantages of the multilevel inverter such as low THD% and high output voltage quality.

VIII. CONCLUSION

A new topology of the three-phase nine-level structure electrical converter was introduced. The recommended configuration was obtained from reduced range of power electronic parts. Therefore, the projected topology ends up in reduction of installation space and value. the elemental frequency stairs modulation technique was well utilized and showed high flexibility and ease au fait. Moreover, the projected configuration was extended to N-level with totally different strategies. what is more, the strategy utilized to work out the magnitudes of the dc voltage provides was well dead. so as to verify the performance of the projected structure electrical converter, the projected configuration was simulated and its epitome was factory-made. The obtained simulation and hardware results met the specified output. Hence, ulterior add the long run might embrace associate extension to higher level with alternative recommended strategies. For purpose of minimizing doctor's degree, a selective harmonic elimination pulse breadth modulation technique are often conjointly enforced.

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