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A New General Topology For Cascaded Multilevel Inverters With Reduced Number Of Components Based On Developed H-Bridge

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***ABSTRACT* -In this paper, a new general cascaded multilevel inverter using developed H-bridges is proposed. The proposed topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies from aforementioned points of view. Moreover, a new algorithm to determine the magnitude of dc voltage sources is proposed. The performance and functional accuracy of the proposed topology using the new algorithm in generating all voltage levels for a 31-level inverter are confirmed by simulation . Also a slightly different topology with 49 level inverter is presented. The difference between the 49 level inverter and the other topology presented in this paper is that without increasing the number of voltage sources the number of levels is increased by increasing the number of switches. The 49 level inverter will be simulated**

***Index Terms*— voltage source inverter, developed H-bridge, multilevel inverter, Cascaded multilevel inverter.**

I. INTRODUCTION

With the advancement in inverters, multilevel inverters have received more attention because high-power and medium voltage ratings provides advantage in of high power quality, lower order harmonics, and better electromagnetic interference etc. By appropriately arranging the semi-conductor based switches the inverter will generate a stepped voltage waveform. The main structures of the multilevel inverters have been presented: “diode clamped multilevel inverter”, “flying capacitor multilevel inverter,” and “cascaded multilevel inverter”. Multilevel inverters is composed of symmetric and asymmetric groups based on the dc voltage sources.

The cascaded multilevel inverter is composed of a number of single-phase H-bridge inverters and is classified into symmetric and asymmetric groups based on the magnitude of dc voltage sources. In the symmetric types, the magnitudes of the dc voltage sources of all H-bridges are equal while in the asymmetric types, the values of the dc voltage sources of all H-bridges are different. In recent years, several topologies with various control techniques have been presented for cascaded multilevel inverters [5]–[8]. In [4] and [9]–[15], different symmetric cascaded multilevel inverters have been presented. The main advantage of all these structures is the low variety of dc voltage sources, which is one of the most important features in determining the cost of the inverter. On the other hand, because some of them use a high number of bidirectional power switches, a high number of insulated gate bipolar transistors (IGBTs) are required, which is the main disadvantage of these topologies. An asymmetric topology has been presented in [16]. The main disadvantage of this structure is related to its bidirectional power switches, which cause an increase in the number of IGBTs and the total cost of the inverter. In [15], a new topology with three algorithms have been presented, which reduce the number of required power switches but increase the variety of dc voltage sources. In [1], [4] and [17], and [18], several algorithms for determining the magnitudes of dc voltage sources for the conventional cascaded multilevel inverter have been presented. The major advantage of this topology and its algorithms is related to its ability to generate a considerable number of output voltage levels by using a low number of dc voltage sources and power switches but the high variety in the magnitude of dc voltage sources is their most remarkable disadvantage. In this paper, in order to increase the number of output

voltage levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of cascaded multilevel inverters is proposed. It is important to note that in the proposed topology, the unidirectional power switches are used. Then, to determine the magnitude of the dc voltage sources, a new algorithm is proposed. Moreover, the proposed topology is compared with other topologies from different points of view such as the number of IGBTs, number of dc voltage sources, the variety of the values of the dc voltage sources, and the value of the blocking voltages per switch. Finally, the performance of the proposed topology in generating all voltage levels through a 49 -level inverter is confirmed by MATLAB simulation.

II. PROPOSEDTOPOLOGY

In Fig. 1, two new topologies are proposed for a seven-level inverter [19]. As shown in Fig. 1, the proposed topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six unidirectional power switches (S_a, S_b, $S_{L,1}$, $S_{L,2}$, $S_{R,1}$, $and\ S_{R,2}$) and two dc voltage sources ($V_{L,1}\ and V_{R,1}$). In this paper, these topologies are called developed H-bridge. As shown in Fig. 1, the simultaneous turn-on of $S_{L,1}\ and\ S_{L,2}$ $(or\ S_{R,1}\ and\ S_{R,2})$

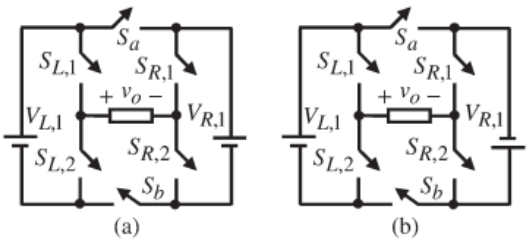


Fig. 1. Proposed seven-level inverters. (a) First proposed topology. (b) Second proposed topology.

No.	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	$v_0(Fig\ .1(a))$	$v_0(Fig\ .1(b))$
1	1	0	0	1	0	1	$V_{L,1}$	$V_{L,1}$
2	1	0	0	1	1	0	$V_{R,1}$	$-V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1} - V_{R,1}$	$V_{L,1} + V_{R,1}$
4	1	0	1	0	1	0	0	0
	0	1	0	1	0	1		
5	0	1	1	0	1	0	$-V_{L,1}$	$-V_{L,1}$
6	0	1	1	0	0	1	$-V_{R,1}$	$V_{R,1}$
7	0	1	0	1	1	0	-$(V_{L,1} - V_{R,1})$	-$(V_{L,1} + V_{R,1})$

causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided. In addition, $S_a$and S_b should not turn on, simultaneously. The difference in the topologies illustrated in Fig. 1 is in the connection of the dc voltage sources polarity. Table I shows the output voltages of the proposed inverters for different states of the switches. In this table, 1 and 0 indicate the $ON-$ and $OFF-$ states of the switches, respectively. As it is obvious from Table I, if the values of the dc voltage sources are equal, the number of voltage levels decreases to three. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources. Considering Table I, to generate all voltage levels (odd and even) in the proposed topology shown in Fig. 1(a), the magnitudes of $V_{L,1}$ and $V_{R,1}$ should be considered $3pu$ and $1pu$, respectively. Similarly, for the topology shown in Fig. 1(a), the magnitudes of $V_{L,1}$ and $V_{R,1}$ should be considered $2pu$ and $1pu$, respectively. Considering the aforementioned explanations, the total cost of the proposed topology in Fig. 1(b) is low because dc voltage sources with low magnitudes are needed. By developing the seven-level inverter shown in Fig. 1(b), the 31-level inverter shown in Fig. 2 can be proposed. This topology consists of ten unidirectional power switches and four dc voltage sources. According to Fig. 2, if the power switches of $(S_{L,1}, S_{L,2})$, $(S_{L,3}, S_{L,4})$, $(S_{R,1}, S_{R,2})$, and $(S_{R,3}, S_{R,4})$ turn on simultaneously, the dc voltage sources of$V_{L,1}, V_{L,2}, V_{R,1}$, and $V_{R,2}$ will be short-circuited, respectively. Therefore, the simultaneous turn-on of these switches should be avoided. In addition, S_a and S_b should not turn on simultaneously. It is important to note that the 31-level topology can be provided through the structure presented in Fig. 1(a), where the only difference will be in the polarity of the applied dc voltage sources. By developing the proposed 31 level inverter, a 127 -level inverter can be proposed as shown in Fig. 3. This topology

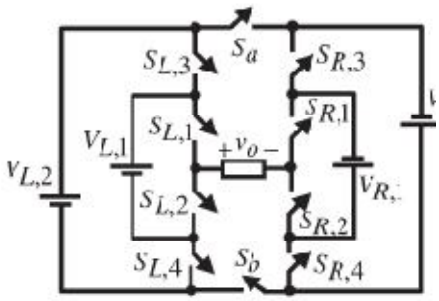


Fig. 2. Proposed 31-level inverter.

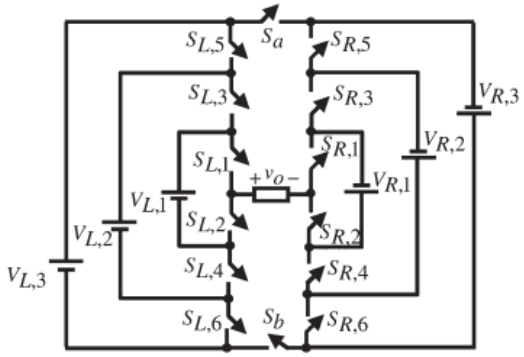


Fig. 3. Proposed 127-level inverter.

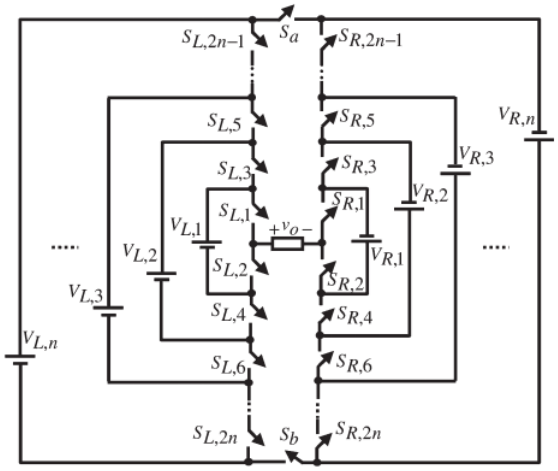


Fig. 4. Proposed general topology.

consists of 14 unidirectional power switches and 6 dc voltage sources. Similarly, by developing the proposed basic topology, a general topology, as shown in Fig. 4, can be proposed. The general topology consists of $2n$ dc voltage sources (n is the number of the dc voltage sources on each leg) and $4n + 2$ unidirectional power switches. In the proposed general topology, the number of output voltage levels(N_{step}), number of switches (N_{switch}), number of dc voltage sources(N_{source}), and the maximum magnitude of the generated voltage ($V_{o,max}$) are calculated as follows, respectively:

$$N_{step} = 2^{2n+1} - 1 \quad \text{---------- (1)}$$

$$N_{switch} = 4n + 2 \quad \text{---------- (2)}$$

$$N_{source} = 2n \quad \text{---------- (3)}$$

$$V_{o,max} = V_{L,n} + V_{R,n} \quad \text{---------- (4)}$$

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values of dc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter's total cost decreases [20]. The number of variety of the values of dc voltage sources $(N_{variety})$is given by

$$N_{variety} = 2n \quad \text{---------- (5)}$$

The following pattern is utilized to calculate the maximum magnitude of the blocking voltage of the power switches. As shown in Fig. 1(b), the blocking voltage of $S_{R,1}$and $S_{R,2}$ are calculated as follows:

$$V_{SR,1} = V_{SR,2} = V_{R,1} \quad \text{---------- (6)}$$

Where $V_{SR,1}$ and $V_{SR,2}$ indicate the maximum blocking voltages of $S_{R,1}$and $S_{R,2}$, respectively. The blocking voltage of $S_{L,1}$and $S_{L,2}$ are as follows:

$$V_{SL,1} = V_{SL,2} = V_{L,1} \quad \text{---------- (7)}$$

Where $V_{SL,1}$and $V_{SL,2}$ indicate the maximum blocking voltages of $S_{L,1}$and $S_{L,2}$, respectively. Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter $(V_{block,1})$is calculated as follows:

$$V_{block,1} = V_{SR,1} + V_{SR,2} + V_{SL,1} + V_{SL,2} + V_{Sa} + V_{Sa} = 4(V_{R,1} + V_{L,1}) \quad \text{---------- (8)}$$

Considering Fig. 2, the maximum blocking voltage of the switches is as follows:

$$V_{SR,1} = V_{SR,2} = V_{R,1} \quad \text{---------- (9)}$$

$$V_{SR,3} = V_{SR,4} = V_{R,2} - V_{R,1} \quad \text{---------- (10)}$$

$$V_{SL,1} = V_{SL,2} = V_{L,1} \quad \text{---------- (11)}$$

$$V_{SL,3} = V_{SL,4} = V_{L,2} - V_{L,1} \quad \text{----------(12)}$$

$$V_{Sa} = V_{Sb} = V_{R,2} + V_{L,2} \quad \text{------- (13)}$$

Therefore, the maximum blocking voltage of all switches of the proposed 31-level inverter($V_{block,2}$)is as follows:

$$V_{block,2} = V_{SR,1} + V_{SR,2} + V_{SR,3} + V_{SR,4} + V_{SL,1} + V_{SL,2} + V_{SL,3} + V_{SL,4} + V_{Sa} + V_{Sb} = 4(V_{R,2} + V_{L,2}) \quad \text{--------- (14)}$$

Similarly, the maximum blocking voltage of all switches of the 49-level inverter is calculated as follows:

$$V_{block,3} = 4(V_{R,3} + V_{L,3}) \quad \text{---------- (15)}$$

Finally, the maximum blocking voltage of all the switches of the general topology $(V_{block,n})$is calculated as follows:

$$V_{block,n} = 4(V_{R,n} + V_{L,n}) \quad \text{---------- (16)}$$

III. PROPOSED ALGORITHM TO DETERMINE THE MAGNITUDES OF DC VOLTAGE SOURCES

In this paper, the following algorithm is applied to determine the magnitude of dc voltage sources. It is important to note that all voltage levels (even and odd) can be generated.

A. Proposed Seven-Level Inverter

The magnitudes of the dc voltage sources of the seven-level inverter shown in Fig. 1(b) are determined as follows:

$V_{L,1} = V_{dc}$ (17)

$V_{R,1} = 2V_{dc}$. (18)

Considering (17), (18), and Table I, the proposed seven-level inverter can generate 0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$ at output

.

B. Proposed 31-Level Inverter

The magnitudes of the dc voltage sources of the proposed 31-level inverter are recommended as follows:

$V_{L,1} = V_{dc}$ (19)

$V_{R,1} = 2V_{dc}$ (20)

$V_{L,2} = 5V_{dc}$ (21)

$V_{R,2} = 10V_{dc}$. (22)

The proposed inverter can generate all negative and positive voltage levels from 0 to $15V_{dc}$ with steps of V_{dc}.

C. Proposed 127-Level Inverter

The magnitudes of the dc voltage sources of the proposed 127-level inverter are calculated as follows:

$$V_{L,1} = V_{dc} \quad \text{---------- (17)}$$

$$V_{R,1} = 2V_{dc} \quad \text{---------- (18)}$$

$$V_{L,2} = 5V_{dc} \quad \text{---------- (19)}$$

$$V_{R,2} = 10V_{dc} \quad \text{---------- (20)}$$

$$V_{L,3} = 25V_{dc} \quad \text{---------- (21)}$$

$$V_{R,3} = 50V_{dc} \quad \text{---------- (22)}$$

By using this algorithm, the inverter can generate all negative and positive voltage levels from 0 to 63 V_{dc} with steps of V_{dc}

D. Proposed General Multilevel Inverter

The magnitudes of the dc voltage sources of the proposed general multilevel inverter can be obtained as follows:

$$V_{Lj} = 5^{j-1}V_{dc} \; for \; j = 1,2,3,\dots,n \quad \text{--------- (23)}$$

$$V_{Rj} = 2 \times 5^{j-1}V_{dc} \; for \; j = 1,2,3,\dots,n \quad \text{---------- (24)}$$

Considering (4) and (16), the values of $V_{o,max}$ and $V_{block,n}$ of the proposed general multilevel inverter are as follows, respectively:

$$V_{o,max} = V_{L,n} + V_{R,n} = 3 \times 5^{n-1}V_{dc} \quad \text{---------- (25)}$$

$$V_{block,n} = 4(V_{L,n} + V_{R,n}) = 12(5^{n-1})V_{dc} \quad \text{---------- (26)}$$

IV. CALCULATION OF LOSSES

Mainly, two kinds of losses (i.e., conduction and switching losses) are associated with the switches. Since the switches include IGBTs and diodes, the conduction losses of an IGBT $(p_{c,IGBT}(t))$ and a diode $(p_{c,D}(t))$ are calculated as follows, respectively [7], [22]:

$$p_{c,IGBT}(t) = [V_{IGBT} + R_{IGBT}i^{\beta}(t)]i(t) \quad \text{---------- (27)}$$

$$p_{c,D}(t) = [V_{IGBT} + R_{IGBT}i^{\beta}(t)]i(t) \quad \text{---------- (28)}$$

Where V_{IGBT} and V_D are the forward voltage drops of the IGBT and diode, respectively. R_{IGBT} and R_D are the equivalent resistances of the IGBT and diode, respectively, and β is a constant related to the specification of the IGBT. Considering that at instant t, there are N_{IGBT} transistors and N_D diodes in the current path, the average value of the conduction

power loss (P_c) of the multilevel inverter can be written as follows:

$$P_c = \frac{1}{2}\int_0^{2\pi} [N_{IGBT}(t)p_{c,T}(t) + N_D(t)p_{c,D}(t)]\, dt$$

---------- (29)

The switching losses are calculated based on the energy loss calculation. The switching losses occur during the turn-off and turn-on periods. For simplicity, the linear variations of the voltage and current of the switches in the switching period are considered. Based on this assumption, the following relations can be written [7], [22]:

$$E_{off,k} = \int_0^{t_{off}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}It_{off}$$

---------- (28)

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \frac{1}{6}V_{sw,k}I't_{on}$$

---------- (29)

Where $E_{off,k}$ and $E_{on,k}$ are the turn-off and turn-on losses of the switch k, respectively. t_{off} and t_{on} are the turn-off and turn-on times of the switch, respectively, I is the current through the switch before turning off, I' is the current through the switch after turning on, and $V_{sw,k}$ is the OFF-state voltage on the switch. The switching power loss (P_{sw}) is equal to the sum of all turn-on and turn-off energy losses in a fundamental cycle of the output voltage. This can be written as follows [7], [22]:

$$P_{sw} = f \sum_{k=1}^{N_{switch}} \left(\sum_{i=1}^{N_{on,k}} E_{on,k_i} + \sum_{i=1}^{N_{off,k}} E_{off,k_i} \right)$$

---------- (30)

Where f is the fundamental frequency and $N_{on,k}$ and $N_{off,k}$ are the numbers of turn-on and turn-off of the switch k during a fundamental cycle. Also, $E_{on,\mathrm{ki}}$ is the energy loss of the switch k during the ith turn-on and $E_{off,ki}$ is the energy loss of the switch k during the ith turn-off. The total loss$(P_{loss})$of the multilevel converter is the sum of the conduction and switching losses as follows:

$$P_{loss} = P_c + P_{sw}$$

-------- (31)

Finally, the efficiency (η) of the inverter is calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}$$

---------- (32)

Where P_{out} and P_{in} denote the output and input powers of the inverter.

V. COMPARING THE PROPOSED GENERAL TOPOLOGY WITH THE CONVENTIONAL TOPOLOGIES

In order to clarify the advantages and disadvantage of the proposed topology, it should be compared with the different kinds of topologies presented in literature. In [4], the conventional cascaded multilevel inverter with two different algorithms has been presented. These algorithms are known as the symmetric cascaded multilevel inverters and the asymmetric ones with the binary method for determining the magnitude of dc voltage sources. In the comparison, the conventional symmetric cascaded multilevel inverter is indicated by R_1 and the conventional binary asymmetric cascaded multilevel inverter is shown by R_2. Three other algorithms have been presented for this topology in [1], [17], and [18], which are indicated by R_3–R_5, respectively. Moreover, another topology with three different algorithms for determining the value of dc voltage sources has been introduced in [15], which are shown by R_{13}–R_{15} in this comparison. In [9]–[12], four different structures for the cascaded multilevel inverter have been presented, and in this paper, they are indicated by R_6–R_7 and R_{11}–R_{12}. It is important to note that the power switches in the aforementioned topologies are unidirectional. In addition, other topologies based on bidirectional switches have been presented in [13] and [14]. In [14], three different algorithms have been recommended, which are denoted as R_8–R_{10}, and the presented topology in [13] is indicated by R_{16} in this comparison. Fig. 5 shows all of the aforementioned structures. Fig. 6 compares the number of IGBTs of the proposed general topology with the aforementioned cascaded multilevel inverters. It is obvious that the proposed inverter requires a lesser number of IGBTs in comparison with the other mentioned topologies to generate particular levels. Fig. 7 compares the number of dc voltage sources of the proposed inverter with the aforementioned cascaded multilevel inverter. As shown in Fig. 7, the proposed inverter has better performance in comparison with the other presented topologies except the topology presented in R_3. However, the magnitude of the dc voltage sources in R_3 is a little more than that of the proposed topology.

Fig. 8 compares the variety of magnitudes of the dc voltage sources of the proposed inverter with that of the aforementioned cascaded multilevel inverter. Obviously, the proposed inverter uses a wider variety of magnitudes of the dc voltage sources in comparison with those of all the aforementioned

topologies. This feature is the most important disadvantage of the proposed topology because the variety of the values of dc voltage sources is as one of the remarkable factors in determining the cost of the inverter. However, this feature in the proposed topology is similar to the presented topologies of R_2 and R_{14}. Fig. 9 compares the magnitude of the blocking voltage of the switches of the proposed inverter with that of the aforementioned cascaded multilevel inverter. This figure shows the reduction of the magnitude of the blocking voltage of the proposed inverter in comparison with those of all the aforementioned multilevel inverters.

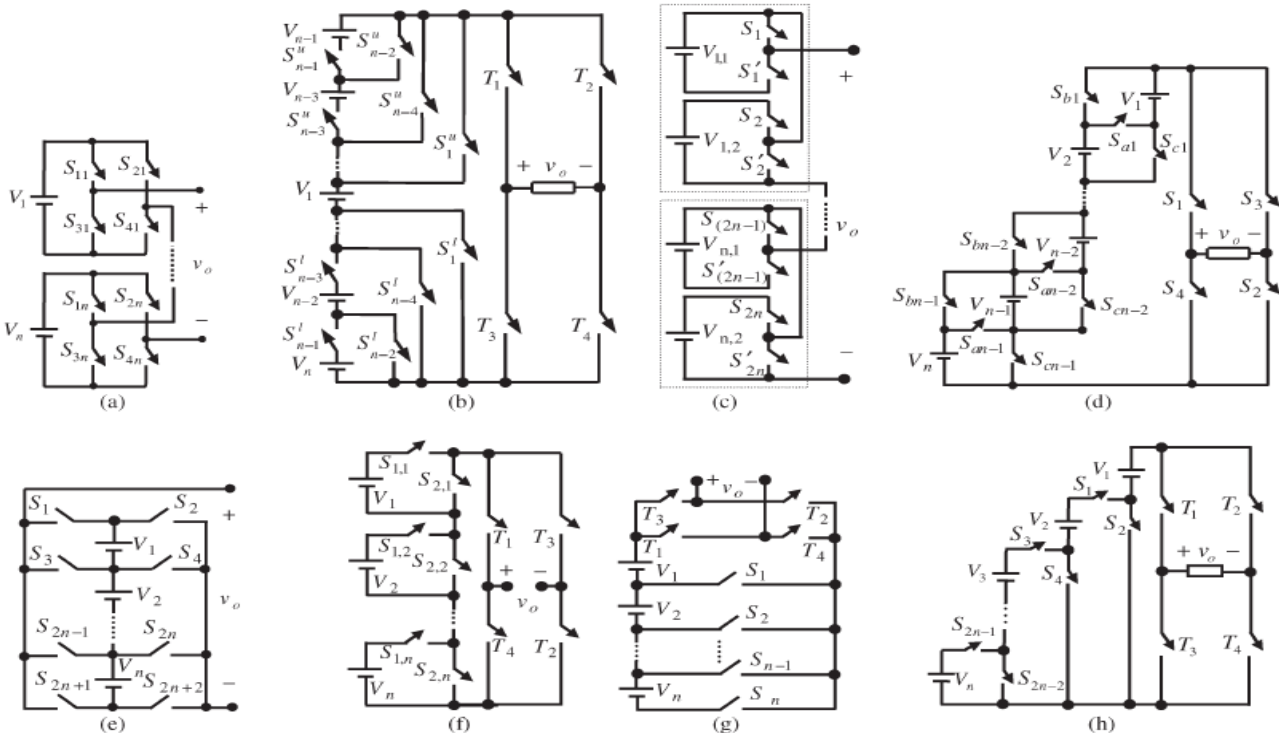


Fig. 5. Cascaded multilevel inverters presented in literature: (a) Conventional cascaded multilevel inverters $R1$ for $V1 = V2 = \cdots = Vn = V\text{dc}$, $R2$ for $V1 = 2j-1V\text{dc}$ ($j = 1, 2, \ldots, n$), $R3$ for $V1 = 3j-1V\text{dc}$ ($j = 1, 2, \ldots, n$), $R4$ for $V1 = 0.5V2 = 0.5V3 = \cdots = 0.5Vn = V\text{dc}$, and $R5$ for $V1 = 2/3 = V3/3 = \cdots = Vn/3 = V\text{dc}$. (b) Presented topology in [12], namely, $R12$ for $V1 = V2 = \cdots = Vn = V\text{dc}$. (c) Presented topology in [10], i.e., $R7$ for $V1 = V2 = \cdots = Vn = V\text{dc}$. (d) Presented topology in [9], i.e., $R6$ for $V1 = V2 = \cdots = Vn = V\text{dc}$. (e) Presented topologies in [14], i.e., $R8$ for $V1 = V2 \cdots = Vn = V\text{dc}$, $R9$ for $V1 = 0.5V2 = 0.5V3 = \cdots = 0.5Vn = V\text{dc}$, and $R10$ for $V1 = 2j-1V\text{dc}$ ($j = 1, 2, \ldots, n$). (f) Presented topologies in [15], i.e. ,$R13$ for $V1 = V2 = \cdots = Vn = V\text{dc}$, $R14$ for $V1 = 2j-1V\text{dc}$ ($j = 1, 2, \ldots, n$), and $R15$ for $V1 = 0.5V2 = 0.5V3 = \cdots = 0.5Vn = V\text{dc}$. (g) Presented topology in [13], i.e., $R16$ for $V1 = V2 = \cdots = Vn = V\text{dc}$. (h) Presented topology in [11], i.e., $R11$ for $V1 = V2 = \cdots = Vn = V\text{dc}$.

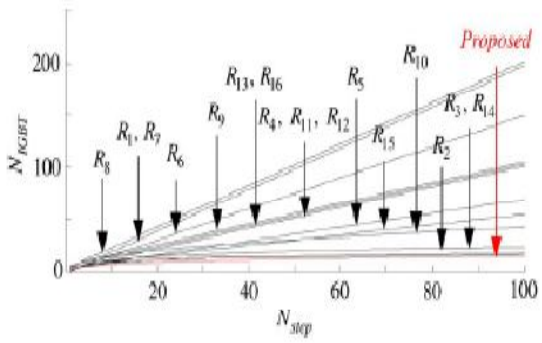


Fig. 6. Variation of N_{IGBT} versus N_{step}.

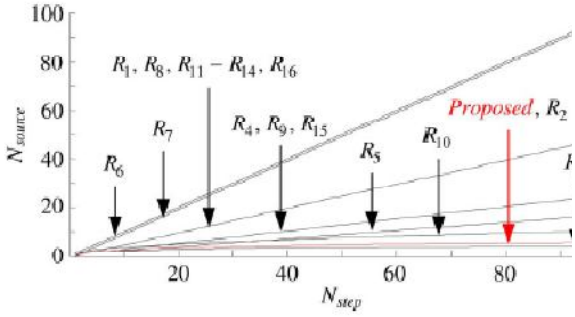


Fig. 7. Variation of N_{source} versus N_{step}.

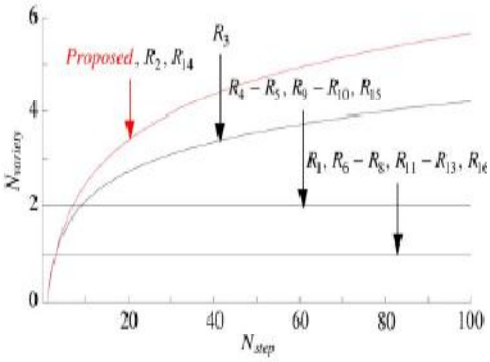


Fig. 8. Variation of $N_{variety}$ versus N_{step}.

Table II
Output voltage of 31 level inverter

No.	SL1	SL2	SL3	SL4	SR1	SR2	SR3	SR4	Sa	Sb	Vo
1	1	0	1	0	1	0	1	0	0	1	$V_{L2}+V_{R2}$
2	0	1	1	0	1	0	1	0	0	1	$V_{L2}+V_{R2}-V_{L1}$
3	1	0	1	0	0	1	1	0	0	1	$V_{R2}+V_{L2}-V_{R1}$
4	0	1	1	0	0	1	1	0	0	1	$V_{L2}+V_{R2}-V_{L1}-V_{R1}$
5	1	0	0	1	1	0	1	0	0	1	$V_{L1}+V_{R2}$
6	0	1	0	1	1	0	1	0	0	1	V_{R2}
7	1	0	0	1	0	1	1	0	0	1	$V_{L1}-V_{R1}+V_{R2}$
8	0	1	0	1	0	1	1	0	0	1	$V_{R2}-V_{R1}$
9	1	0	1	0	1	0	0	1	0	1	$V_{L2}+V_{R1}$
10	0	1	1	0	1	0	0	1	0	1	$V_{L2}+V_{R1}-V_{L1}$
11	1	0	1	0	0	1	0	1	0	1	V_{L2}
12	0	1	1	0	0	1	0	1	0	1	$V_{L2}-V_{L1}$
13	1	0	0	1	1	0	0	1	0	1	$V_{L1}+V_{R1}$
14	0	1	0	1	1	0	0	1	0	1	V_{R1}
15	1	0	0	1	0	1	0	1	0	1	V_{L1}
16	1	0	1	0	1	0	1	0	1	0	0
17	0	1	1	0	1	0	1	0	1	0	$-V_{L1}$
18	1	0	1	0	0	1	1	0	1	0	$-V_{R1}$
19	0	1	1	0	0	1	1	0	1	0	$-(V_{L1}+V_{R1})$
20	1	0	0	1	1	0	1	0	1	0	$-(V_{L2}-V_{L1})$
21	0	1	0	1	1	0	1	0	1	0	$-V_{L2}$
22	1	0	0	1	0	1	1	0	1	0	$-(V_{L2}+V_{R1}-V_{L1})$
23	0	1	0	1	0	1	1	0	1	0	$-(V_{L2}+V_{R1})$
24	1	0	1	0	1	0	0	1	1	0	$-(V_{R2}-V_{R1})$
25	0	1	1	0	1	0	0	1	1	0	$-(V_{L1}-V_{R1}+V_{R2})$
26	1	0	1	0	0	1	0	1	1	0	$-V_{R2}$
27	0	1	1	0	0	1	0	1	1	0	$-(V_{L1}+V_{R2})$
28	1	0	0	1	1	0	0	1	1	0	$-(V_{L2}+V_{R2}-V_{L1}-V_{R1})$
29	0	1	0	1	1	0	0	1	1	0	$-(V_{R2}+V_{L2}-V_{R1})$
30	1	0	0	1	0	1	0	1	1	0	$-V_{L2}+V_{R2}-V_{L1}$
31	0	1	0	1	0	1	0	1	1	0	$-(V_{L2}+V_{R2})$

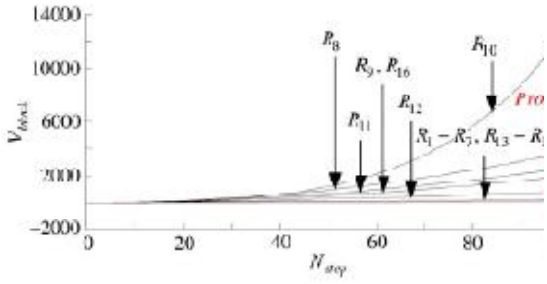


Fig. 9. Variation of V_{block} versus N_{step}.

VI. SIMULATION RESULTS

In order to verify the correct performance of the proposed multilevel inverter in generating all output voltage levels (even and odd), a 31-level inverter based on the topology shown in Fig. 2 has been used for the simulation. Table II shows the switching states of the 31-level inverter.

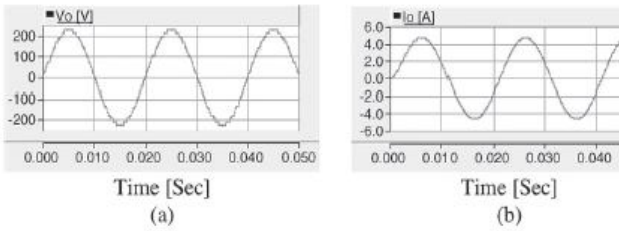
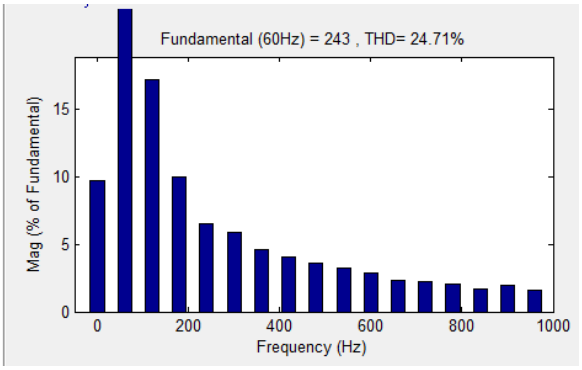
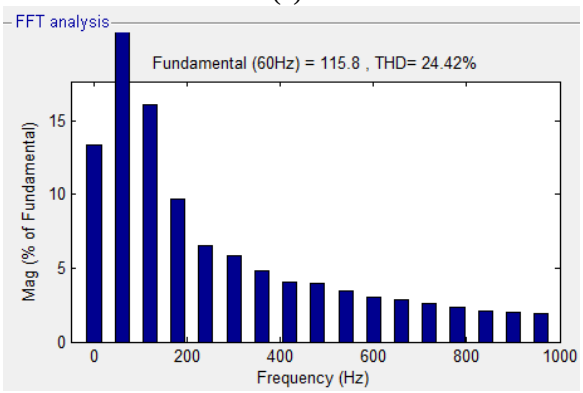


Fig. 11. Proposed 31-level inverter. (a) Output voltage waveform. (b) current waveform.

The simulation is done by using PSCAD software. According to 31level inverter, the maximum output voltage of this inverter will be 225 V. In this paper, the fundamental frequency switching control method has been used [21]. In this method, the sinusoidal reference voltage is compared with the available dc voltage levels and the level that is nearest to the reference voltage is chosen [22]. The main advantage of this control method is related to its low switching frequency, which leads to reduction of switching losses. The simulated output voltage and current waveforms are shown in Fig. 11. As Fig. 11(a) shows, the proposed topology is able to generate 31 levels (15 positive levels, 15 negative levels, and 1 zero level) with the maximum voltage of 225 V. Comparing the output voltage and current waveforms indicates that the output current waveform is more similar to the ideal sinusoidal waveform than the output voltage because the R–L load acts as a low-pass filter. In addition, there is a phase difference between the output voltage and current waveforms, which is caused by the inductive feature of the load. The total harmonic distortions of the output voltage and current are equal to 0.94% and 0.19%, respectively. Fig. 12(a) and (b) shows the harmonic spectrum of the output voltage and current, respectively. The figure shows that the magnitudes of harmonics of both voltage and current waveforms are low. However, the harmonics of the current waveform are lower than the voltage



(a)



(b)

Fig. 12. Harmonic spectrum of (a) output voltage and (b) current.

waveform. It is important to note that in Fig. 12, in order to show the magnitudes of the fundamental and high-order harmonics, the scale of the vertical axis is considered nonlinear. In the test condition, the measured input and output powers are about 1203 and 1112 W, respectively. Therefore, the efficiency is about 92.4%. Based on the loss calculations given before, the power loss is about 86 W. Therefore, the calculated loss has a good accordance with the measured efficiency. As mentioned before, the power switches in the proposed topology are unidirectional from the voltage viewpoint. In order to prove this issue, the voltages on the switches of a single leg of the inverter $(i.e., S_{L,1}, S_{L,2}, S_{L,3}, S_{L,4}, and\ S_a)$ are

shown in Fig. 13. As can be seen, the maximum blocking voltage by switches $S_{L,1}, S_{L,2}, S_{L,3}, S_{L,4}$, *and* S_a are equal to 15, 15, 60, 60, and 225 V, respectively. Obviously, the voltage values are zero or equal to the positive ones, which is well in accordance to the unidirectional feature of the switches from the voltage view point. Considering the magnitude of the blocking voltage of the switches, the relations associated to the maximum voltage drop of the switches are well confirmed.

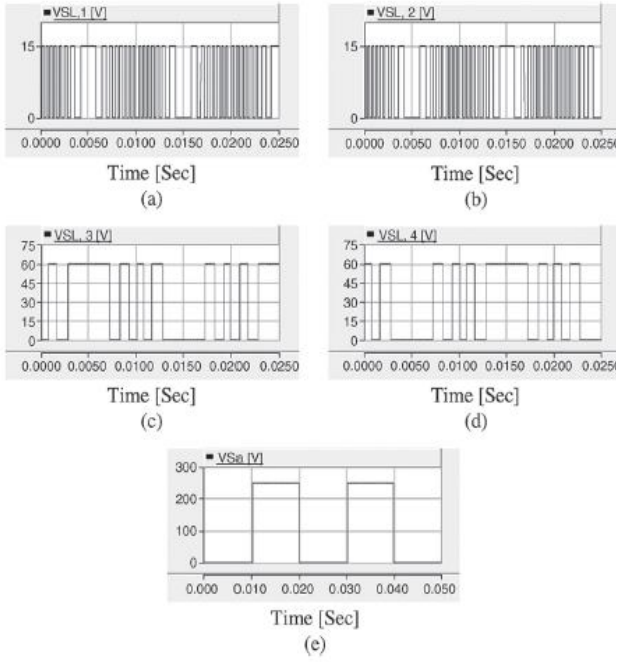


Fig. 13. Voltages of switches (a) $S_{L,1}$, (b) $S_{L,2}$, (c) $S_{L,3}$, (d) $S_{L,4}$, an (e) S_a.

49 Level Inverter

The 49 level inverter has the same number of voltage sources as that of 31 level inverter presented in these paper. However it has two more switches. So in this case we have increased the number of voltage levels by increasing the number of switches, without increasing the number of voltage sources. The switches for the 49 level inverter are SL11, SL12, SR11, SR12, SL21, SL22, SR21,SR22, Sa1,Sb1,Sa2 and Sb2. So here the number of switches is 12 compared to 10 for 31 level inverter.

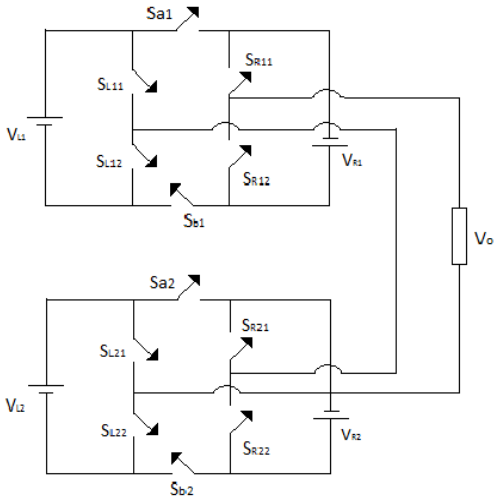


Fig14. Proposed 49 level inverter

No.	SL11	SL12	SR11	SR12	Sa1	Sb1	SL21	SL22	SR21	SR22	Sa2	Sb2	Vo
1	1	0	0	1	0	1	1	0	0	1	0	1	VL1+ VL2
2	1	0	0	1	0	1	1	0	0	1	1	0	VL1-VR2
3	1	0	0	1	0	1	1	0	1	0	0	1	VL1+VL2+VR2
4	1	0	0	1	0	1	1	0	1	0	1	0	VL1
5	1	0	0	1	0	1	0	1	1	0	1	0	VL1-VL2
6	1	0	0	1	0	1	0	1	1	0	0	1	VL1+VR2
7	1	0	0	1	0	1	0	0	1	0	1	10	VL1-VL2-VR2
8	1	0	0	1	1	0	1	0	0	1	0	1	-VR1+VL2
9	1	0	0	1	1	0	1	0	0	1	1	0	-(VR1+VR2)
10	1	0	0	1	1	0	1	0	1	0	0	1	-VR1+VL2+VR2
11	1	0	0	1	1	0	1	0	1	0	1	0	-VR1

12	1	0	0	1	1	0	0	1	1	0	1	0	-VR1-VL2
13	1	0	0	1	1	0	0	1	1	0	0	1	-VR1+VR2
14	1	0	0	1	1	0	0	1	0	1	1	0	-(VR1+VL2+VR2)
15	1	0	1	0	0	1	1	0	0	1	0	1	VL1+VR1+VL2
16	1	0	1	0	0	1	1	0	0	1	1	0	VL1+VR1-VR2
17	1	0	1	0	0	1	1	0	1	0	0	1	VL1+VR1+VL2+VR2
18	1	0	1	0	0	1	1	0	1	0	1	0	VL1+VR1
19	1	0	1	0	0	1	0	1	1	0	1	0	VL1+VR1-VL2
20	1	0	1	0	0	1	0	1	1	0	0	1	VL1+VR1+VR2
21	1	0	1	0	0	1	0	1	0	1	1	0	VL1+VR1-VL2-VR2
22	1	0	1	0	1	0	1	0	0	1	0	1	VL2
23	1	0	1	0	1	0	1	0	0	1	1	0	-VR2
24	1	0	1	0	1	0	1	0	1	0	0	1	VL2+VR2
25	1	0	1	0	1	0	1	0	1	0	1	0	0

No.	SL11	SL12	SR11	SR12	Sa1	Sb1	SL21	SL22	SR21	SR22	Sa2	Sb2	Vo
26	1	0	1	0	1	0	0	1	1	0	1	0	-VL2
27	1	0	1	0	1	0	0	1	1	0	0	1	VR2
28	1	0	1	0	1	0	0	1	0	1	1	0	-(VL2+VR2)
29	0	1	1	0	1	0	1	0	0	1	0	1	-VL1+VL2
30	0	1	1	0	1	0	1	0	0	1	1	0	-VL1-VR2
31	0	1	1	0	1	0	1	0	1	0	0	1	-VL1+VL2+VR2
32	0	1	1	0	1	0	1	0	1	0	1	0	-VL1
33	0	1	1	0	1	0	0	1	1	0	1	0	-VL1-VL2
34	0	1	1	0	1	0	0	1	1	0	0	1	-VL1+VR2
35	0	1	1	0	1	0	0	1	0	1	1	0	-VL1-(VL2+VR2)
36	0	1	1	0	0	1	1	0	0	1	0	1	VR1+VL2
37	0	1	1	0	0	1	1	0	0	1	1	0	VR1-VR2
38	0	1	1	0	0	1	1	0	1	0	0	1	VR1+VL2+VR2
39	0	1	1	0	0	1	1	0	1	0	1	0	VR1
40	0	1	1	0	0	1	0	1	1	0	1	0	VR1-VL2
41	0	1	1	0	0	1	0	1	1	0	0	1	VR1+VR2
42	0	1	1	0	0	1	0	1	0	1	1	0	VR1-(VL2+VR2)
43	0	1	0	1	1	0	1	0	0	1	0	1	-(VL1+VR1)+VL2
44	0	1	0	1	1	0	1	0	0	1	1	0	-(VL1+VR1)-VR2
45	0	1	0	1	1	0	1	0	1	0	0	1	-(VL1+VR1)+VL2+VR2
46	0	1	0	1	1	0	1	0	1	0	1	0	-(VL1+VR1)
47	0	1	0	1	1	0	0	1	1	0	1	0	-(VL1+VR1)-VL1
48	0	1	0	1	1	0	0	1	1	0	0	1	-(VL1+VR1)+VR1
49	0	1	0	1	1	0	0	1	0	1	1	0	-(VL1+VR1)-(VL2+VR2)

The 49 level inverter can be understood more clearly if we think it as two 7 level inverters connected in series. But the main difference is that the output voltage or load is connected as shown in the figure 14. Whereas in case of seven level inverter the output voltage is connected in the middle of the

circuit as shown in its figure. Here in 49 level inverter the magnitude of voltages sources are VL1= 10V, VL2=70V, VR1=20V and VR2=140V. The maximum voltage output is 240V. The 49 level inverter is basically two cascaded 7 level inverters, therefore its output is the sum of the two cascaded inverters. Lets us take that Vo1 is the output voltage of first seven level inverter and Vo2 is the output voltage of second seven level inverter, then the output of the 49 level inverter will be Vo1+ Vo2 . Keeping this in mind we can form the output table of the 49 level inverter as shown in Table III.

CONCLUSION

In this paper, two basic topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 31-level, 127-level, and general topologies are consequently presented. In addition, a new algorithm to determine the magnitude of the dc voltage sources has been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison results, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. However, the proposed topology has a higher number of variety of dc voltage sources in comparison with the others. The performance accuracy of the proposed topology was verified through the PSCAD simulation and the experimental results of a 31-level inverter. Also a 49 level inverter with 12 swithces is proposed which has the same number of voltage sources as that of 31 level inverter to show that the number of levels can be increased without increasing the number of voltage sources. The same was verified through simulation.

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