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DESIGN OF LOW-POWER RECONFIGURABLE 32X32 BIT MULTIPRECISION VOLTAGE SCALING MULTIPLIER

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Abstract: In this paper, we present flexible multi-precision multiplier that combined variable precision, parallel processing (PP), razor based dynamic voltage scaling (DVS), and dedicated MP operand scheduling to provide optimum performance for variety of operating conditions. All of the building blocks of proposed flexible multiplier can either work as independent small precision multiplier or parallel to perform higher-precision multiplier. While still maintain full through-put, the dynamic voltage and frequency scaling management unit configures the multiplier to operate at the proper precision and frequency. Adapting to the run-time workload for targeted application, that flexible multiplier can used to design IIR filter for DSP application. Razor flip-flops together with a dithering voltage unit then configure the multiplier to achieve the lowest power consumption. The single-switch dithering voltage unit and razor flip-flops help to reduce the voltage margin and over head typically associated to DVS to lowest level. Finally, the proposed high speed flexible multiplier can further benefits from an operand scheduler that rearranges the input data, hence determine the optimum voltage and frequency operating conditions for minimum for power consumption.

Keywords- Computer arithmetic, dynamic voltage scaling, low power design, multi-precision multiplier.

I. Introduction

Consumer demand for increasingly portable yet high performance multimedia and communication products impose stringent constraints on the power consumption of individual internal components of these multiplier perform one of the most frequently encountered arithmetic operation in digital signal processor. Multiplier is typically designed for a fixed maximum word-length to suit the worst case scenario. However, the real effective word-lengths of an application vary dramatically. The use of a non-proper word length may cause performance degradation or inefficient usage of the hardware resources. In addition, the minimization of the multiplier power budget requires the estimation of the optimal operating point including clock frequencies, supply voltage, and threshold voltage.In most VLSI system designs, the supply voltage is also selected based on the worst case scenario. In order to achieve an optimal power/performance ratio, a variable precision data path solution is needed to cater for various types of applications. Dynamic Voltage Scaling (DVS) can be used to match the circuit's real working load and further reduce the power consumption. Given their fairly complex structure and interconnections, multiplier can exhibits a large number of unbalanced paths, resulting in substantial glitch generation and propagation.This spurious switching activity can be mitigated by balancing internal paths through a combination of architectural and transistor-level Optimization techniques .Several works investigated this word-length optimization of proposed multiplier of different precision, with each pair of incoming operands is routed to the smallest multiplier that can compute the result to take advantage of the

lower energy consumption of the smaller circuit. This ensemble of point systems is reported to consume the least power but this came at cost increased chip area given the used ensemble structure. To address this issue, proposed to share and reuse some functional modules within the ensemble, an 8-bit multiplier is reused for the 16-bit multiplication adding scalability with out large area penalty. A more flexible approach is proposed by Combining multi-precision (MP) with dynamic voltage scaling (DVS) can provide a dramatic reduction in power consumption by adjusting the supply voltage according to Circuit's run-time workload rather than fixing it to cater for the worst case scenario. when adjusting the voltage, the actual performance of multiplier running under scaled voltage has to be characterized to guarantee a fail-safe operation. Conventional DVS technique consist mainly of lookup table (LUT) the LUT approach tune the supply voltage according to predefined voltage frequency relationship stored in a LUT, which is formed worst case condition(process variation, power supply voltage droops, noise many more) therefore, large margin are necessarily added, which in turn necessary decrease effectiveness of DVS technique. Therefore, voltage could be scaled to the extent that the replica fails to meet the timing. However, safety margins are still needed to compensate for the delay mismatch and address fast-changing transient effects .the aforementioned limitation of conventional DVS techniques motivated recent research efforts into error-tolerant DVS approaches , which can run-time operate the circuit even at a voltage level at which timing error occur, A recovery mechanism is then applied to detect and correct data. Because completely remove safety margins, error- tolerant DVS techniques can further aggressively reduce power consumption. In this paper, we propose a low power reconfigurable multiplier architecture that combined MP with an error-tolerant DVS approach based on razor flip-flops, the main contributions of this paper can be summarized follows. Silicon area is optimized by apply reduction technique that replace a multiplier by adders/subtractors. a silicon implementation of this multi-precision multiplier integrating error tolerant razor based dynamic DVS approach. The run–time adaption to actual workload condition and allow minimum supply voltage and frequency, while meet throughput operation. A dedicated operand scheduler that rearrange operation on input operands so as to reduce the number of transitions of the supply voltage and, in turn, minimize the overall power consumption of the flexible multi-precision multiplier.

A multiplier is an important part of digital signal processing systems, like frequency domain filtering (FIR and IIR), frequency-time transformations (FFT), Correlation, Digital Image processing etc. Multipliers have large area, long latency and consume considerable power. While many previous works focused on implementing high-speed multipliers, recently there have been many attempts to reduce power consumption. This is due to the increased demand for portable multimedia applications, which require low power consumption as well as high speed, they are classified as serial, parallel and serial-parallel multipliers.

In parallel multipliers, there are two main classifications. They are array and tree multipliers. Tree multipliers add as many partial products in parallel as possible and therefore, are very high performance architecture. Unfortunately tree multipliers are very irregular, hard to layout and hence large. Array multipliers, on the other hand, are very regular, small in size but suffer in latency and propagation delay. Booth multiplier is used for signed binary numbers. They are also called radix-2 multiplier. Their main advantage is that it involves no correlation cycles for signed terms. But they become inefficient for alternate zeros and ones as it involves large numbers of adders and subtractors, his result in area and speed limitation. The problem is overcome with modified booth multiplier (MBM) or radix-4 multiplier which reduces the partial products by 50%. Thus it improves speed, reduce power consumption and also save multiplier layout area. MBM also has a regular structure.

II. System Overview and Operation

The proposed MP multiplier system (Fig. 1) comprises five different modules that are as follows:
1) The MP multiplier;
2)The input operands scheduler (IOS) whose function is to reorder the input data stream into a buffer, hence to reduce the required power supply voltage transitions.
3)The frequency scaling unit implemented using a voltage controlled oscillator (VCO). Its function is to generate the required operating frequency of the multiplier;
4)The voltage scaling unit (VSU) implemented using a voltage dithering technique to limit silicon area overhead. Its function is to dynamically generate the supply voltage so as to minimize power consumption;
5)The dynamic voltage/frequency management unit(VFMU) that receives the user requirements (e.g., throughput).

The VFMU sends control signals to the VSU and FSU to generate the required power supply voltage and clock frequency for the MP multiplier.

The MP multiplier is responsible for all computations. It is equipped with razor flip-flops that can report timing errors associated to insufficiently high voltage supply levels.The operation principle is as follows. Initially, the multiplier operates at a standard supply voltage of 3.3 V. If the razor flipflops of the multiplier do not report any errors, this means that the supply voltage can be reduced. This is achieved through the VFMU, which sends control signals to the VSU, hence to lower the supply voltage level. When the feedback provided by the razor flip-flops indicates timing errors, the scaling of the power supply is stopped.

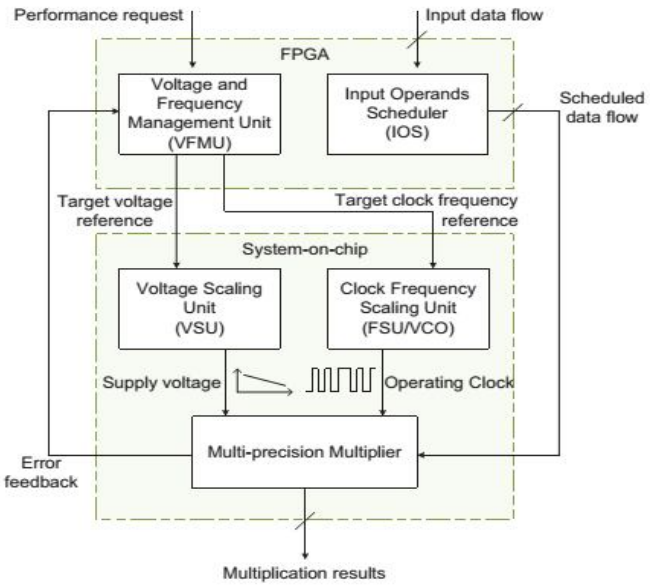


Fig.1: Overall multiplier system architecture.

MP multiplier

The proposed multiplier (Fig.2) not only combines MP and DVS but also parallel processing (PP). Our multiplier comprises 8×8 bit reconfigurable multipliers. These building blocks can either work as nine independent multipliers or work in parallel to perform one, two or three 16×16 bit multiplications or a single 32×32 bit operation. PP can be used to increase the throughput or reduce the supply voltage level for low power operation.

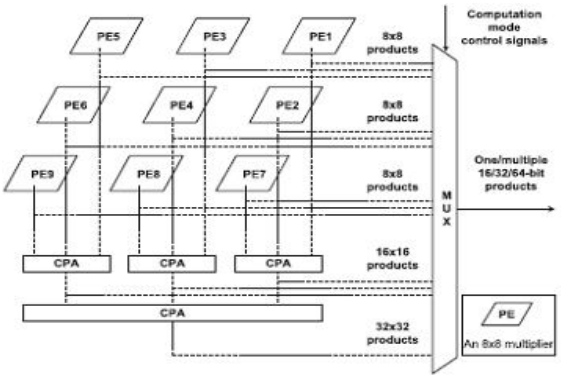


Fig.2: Possible configuration modes of existing MP multiplier

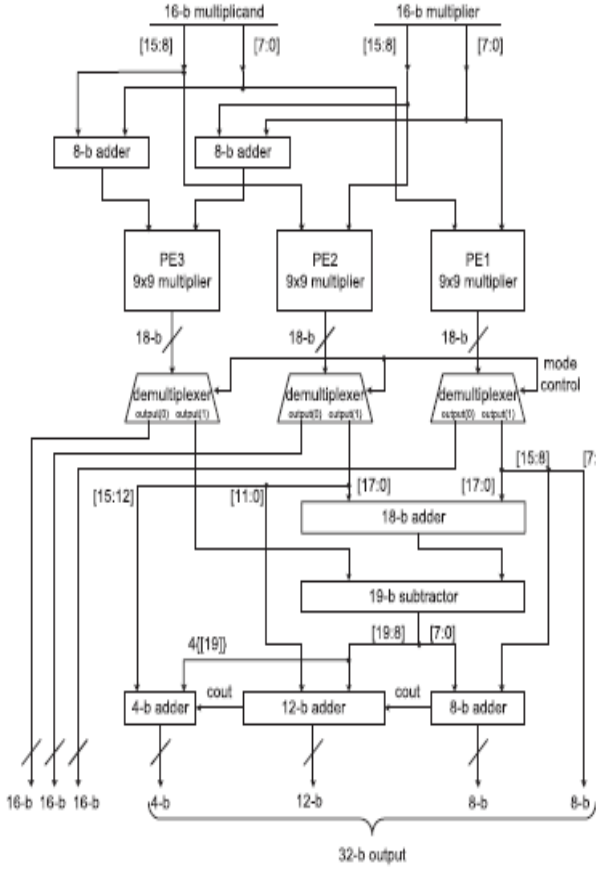


Fig.3 : Three PEs combined to form 16 x 16 bit multiplier

To evaluate the overhead associated to reconfigurability and MP, we define **X** and **Y** as the 2*n*-bits wide multiplicand and multiplier, respectively. $\mathbf{X}_H$, $\mathbf{Y}_H$ are their respective *n* most significant bits whereas $\mathbf{X_L}$,$\mathbf{Y_L}$ are their respective *n* least significant bits. $\mathbf{X_L}\,\mathbf{Y_L}$, $\mathbf{X_H}\,\mathbf{Y_L}$, $\mathbf{X}_L\,\mathbf{Y_H}$, $\mathbf{X}_H\,\mathbf{Y_H}$ is the crosswise products. The product of **X** and **Y** can be expressed as follows:

$$P = (X_H Y_H)2^{2n} + (X_H Y_L + X_L Y_H)2^n + X_L Y_L \quad \text{.....} \quad (1) \qquad \textbf{(1)}$$

where 2*n*-bit reconfigurable multiplier can be built using adders and four *n* bit × *n* bit multipliers to compute $\mathbf{X}_H\,\mathbf{Y_H}$, $\mathbf{X}_H\,\mathbf{Y_L}$, $\mathbf{X}_L\,\mathbf{Y_H}$, and $\mathbf{X}_L\,\mathbf{Y_L}$. we define

$$X' = X_H + X_L \quad \text{...} \quad (2)$$

$$Y' = Y_H + Y_L \quad \text{...} \quad (3)$$

then (1) could be rewritten as follows:

$$P = (X_H Y_H)2^{2n} + (X' Y' - X_H Y_H - X_L Y_L)2^n + X_L Y_L \quad \text{.} \quad \text{.....} \quad (4)$$

Comparing (1) and (4), we have removed one n × *n* bit multiplier (for calculating $\mathbf{X}_H\,\mathbf{Y_L}$ or $\mathbf{X}_L\,\mathbf{Y_H}$) and one 2*n*-bit adder (for calculating $\mathbf{X}_H\,\mathbf{Y_L} + \mathbf{X}_L\,\mathbf{Y_H}$). The two adders are replaced with two n-bit adders (for calculating $\mathbf{X_H}+\mathbf{X_L}$ and $\mathbf{Y_H}+\mathbf{Y_L}$) and two (2n+n)-bit subtractors (for calculating $\mathbf{X'\,Y'} - \mathbf{X}_H\,\mathbf{Y_H} - \mathbf{X}_L\,\mathbf{Y_L}$) .In a 32 bit multiplier , we can thus significantly reduce the design complexity by using two 32-bit subtractors to replace a 16x16 bit multiplier.We actually need two 16x16 bit multiplier (for calculating $\mathbf{X}_H\,\mathbf{Y_H}$ and $\mathbf{X}_L\,\mathbf{Y_L}$) and one 17x17 bit multipliers (for calculating $\mathbf{X'\,Y'}$)

Dynamic voltage and Frequency Scaling Management

A. Dynamic Voltage Scaling (DVS) unit

In this implementation DVS unit shows a dynamic power supply and a VCO are employed to achieve real-time dynamic voltage and scaling can be achieved when using voltage dithering, which exhibits faster response time than conventional voltage regulator. Voltage dithering uses power switches to connect different supply voltage to the load, depending on the time slots. Therefore, an intermediate average voltage is achieved.

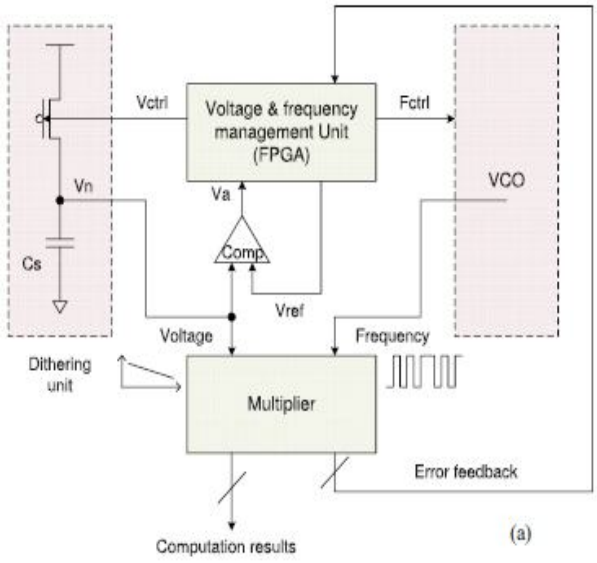


Fig.4: Proposed single-header voltage dithering unit

B. Dynamic Frequency Scaling Unit

In the proposed 32 ×32 bit MP multiplier, dynamic frequency tuning is used to meet throughput requirements. It is based on a VCO implemented as a seven-stage current starved ring oscillator. The VCO output frequency can be tuned from 5 to 50 MHz using four control bits (5 MHz/step).This frequency range is selected to meet the requirements of general purpose DSP applications. The reported multiplier can operate as a 32-bit multiplier or as nine independent 8-bit multipliers. For the chosen 5–50 MHz operating range, our multiplier boasts up to 9 ×50 =450 MIPS. The simulated power consumption for the VCO ranges from 85 (5 MHz) to 149μW (50 MHz), which is negligible compared with the power consumed by the multiplier. Fig. 7 shows experimental measurements showing the transient response for the worst case frequency switching (from 50 to 5 MHz). Clock frequency can settle within one clock cycle as required.

Implementation of Razor Flip-Flops

Although the worst case paths are very rarely exercised, traditional DVS approaches still maintain relatively large safety margins to ensure reliable circuit operation, result in excessive power dissipated. The razor technology is breakthrough work, which eliminates the safety margin by achieving variable tolerance through in-situ error detection and correction ability . This approach is based on a razor flip-flops, which detects and correct the delay error by double sampling.

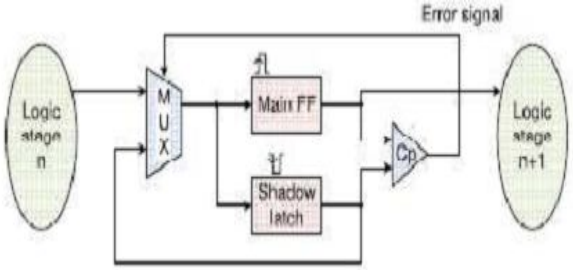


Fig.5: Conceptual view of razor flip-flops

The razor flip-flops are constructed out of a standard positive Edge triggered flip-flops (DFF) augmented with a shadow latch which samples at the negative clock edge. Thus, the input data is given additional time, equal to the duration of the positive clock phase, to settle down to its correct state before being sampled by the shadow latch. In order to ensure the shadow latch always capture the correct data, the minimum allowable supply voltage needs to be constrained during design time such that step-up time at the shadow latch. A comparator flags a timing error when it detects a discrepancy between the speculative sampled at the main flip-flops and the correct data sampled at the shadow latch.

Fig. 1 shows that a global error signal is fed to the VFMU so as to alert the controlling unit whenever the current operating voltage is lower than necessary. The VFMU will then increase the voltage reference. This will in turn result in the VSU generating a new supply voltage level based on the new target voltage reference. When an error occurs, results can be recomputed at any pipeline stage using the corresponding input of the shadow latch. Therefore, the correct values can be forwarded to the corresponding next stages The actual implementation of razor flip-flops requires careful design to meet timing constraints and avoid system failure.

Input Operand Scheduler Unit

1. Motivation and Operation Principle

Main motivation and operating principle of input operand scheduler that rearranges operations on input operands so as to reduces the number of transition of the supply voltage and, in turn, minimize the overall power consumption of the multiplier. Whose function is reordering the input data stream into a buffer, hence to reduce the required power supply voltage transitions. The multiplier provide three different precision modes (32×32bit, 16×16, 8×8-bits), the supply voltage would to transit dynamically between the minimum required voltage levels Vmin32, Vmin16, Vmin8, required for 32, 16, 8-bit operands, respectively, we propose an IOS that will perform following task:

1. Reorder the input data stream such that same precision operands are grouped together into a buffer.

2. Find the minimum supply voltages (Vmin32, Vmin16, Vmin8), and operating frequencies (f32,f16, f8) for three different-precision data grouped to minimize the overall power consumption while still meeting the specified throughput.

$$P_{\text{computation}} = C_m V_{\min}{}^2 f$$

Where Cm is the effective capacitance of the multiplier, Vmin is the applied minimum supply voltage, and f is the applied operating frequency.

2. Algorithm A

In the first algorithm, the multiplier throughput Tp=64 F is kept constant by fixing the operating frequencies (f32, f16, or f8) of each precision-data group (32, 16, or 8bit) to

$$f_{32} = F,\ f_{16} = \frac{F}{2},\ f_8 = \frac{F}{4}$$

Where F is the multiplier's operating frequency.The through put in 8×8 bit multiplication mode is four times that of the 32 ×32 bit multiplication mode and double that of the 16 ×16 bit multiplication mode, as a result of the multiplier PP. The minimum supply voltage (Vmin32, Vmin16 or Vmin8) associated to each operating frequency (f32, f16 or f8) is determined through a Vmin–f LUT.

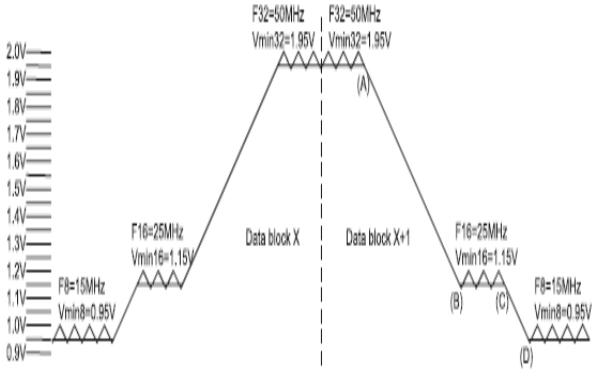


Fig.6 : Algorithm A

Algorithm A shows its limitations when 32-bit operands are processed initially. When all N32 operands of the data block are processed, the supply voltage needs to decrease rapidly from point A (Vmin32) to point B (Vmin16) at which all N16 16-bit operands of the data block should be processed. If N16 is too small, most 16-bit operands will be actually processed in Sections A and B, that is at a voltage possibly much higher than the minimal Vmin16 level. Similarly 8-bit operands of the data block could be processed in Sections C and D, B-C, or even A-B for the worst case. Compared with the fixed width 32×32 bit standard multiplier (32×32 bit mode must be chosen given that a third of operands are 32-bit), 77.7% total power reduction is achieved with a total silicon area overhead of only 11.1%, when considering DVS, razor, RAM, and dedicated circuitry for scheduling algorithm A.

3. Algorithm B

This algorithm removes all transitions of the power supply voltage by makingVmin32, Vmin16 and Vmin8 equal and adjusting f32, f16,and f8 such that the overall throughput is kept unchanged.

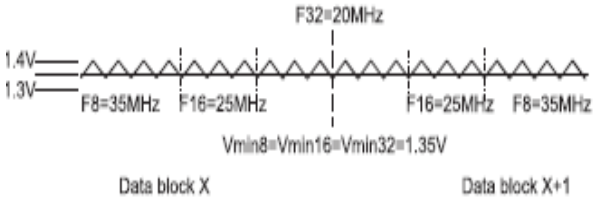


Fig.7 : Algorithm B

From LUT , we can obtain the Vmin – f relationship as follows:

$$V_{min32} = \psi_{32}(f_{32})$$
$$V_{min16} = \psi_{16}(f_{16})$$
$$V_{min8} = \psi_{8}(f_{8}).$$

As algorithm B keeps the supply voltage constant

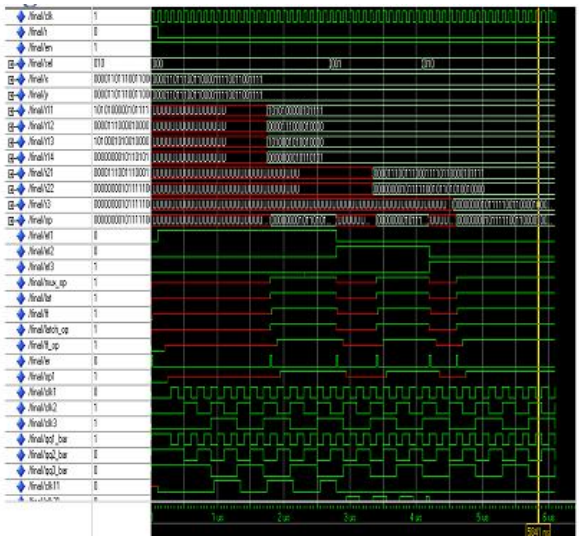
$$\psi_{32}(f_{32}) = \psi_{16}(f_{16}) = \psi_{8}(f_{8}) = V$$

Due to the complete removal of voltage transitions, the Pcompu_overhead is reduced. Simultaneously, because of holistic planning, the dynamic computation power is also optimized to a lower level. Compared with the fixed-width 32×32 bit standard multiplier, 81.5% power reduction is achieved with a total silicon area overhead of only 11.9%, when considering DVS, razor, RAM, and dedicated circuitry for scheduling Algorithm B.

4. Algorithm C

Although Algorithm B removes power supply voltage transitions by setting a single-voltage level V, there may be better power saving combinations of power supply voltages and operating frequencies: (Vmin32, f32), (Vmin16, f16), and (Vmin8, f8). The aim of algorithm C is to find such an optimum for reduced power consumption.

III. Simulation Result of MP Multiplier :



shows the simulation result of multiprecision reconfigurable multiplier, in which dynamic voltage scaling and razor based error detection unit is used to provide full computational flexibility and low power application

IV. Conclusion

In this paper a flexible multiplier combining variable precision processing, scaled voltage and clock frequency are used efficiently to reduce circuit power consumption. Various algorithms are explored to obtain high performance. Reported result show that variable precision multiplier enables a reduction of power dissipation compared to fixed precision multiplier. When operating under different precision, the multi-precision multiplier is used in attractive various general purpose low power application. Related work multi-precision multiplier can be implemented using high speed adders such as carry select adder for improving the performance of high speed flexible multiplier for design IIR filter application.

V. References

[1] R. Min, M. Bhardwaj, S.-H. Cho, N. Ickes, E. Shih, A. Sinha, A. Wang,and A. Chandrakasan, "Energy-centric enabling technologies for wireless sensor networks," IEEE Wirel. Commun., vol. 9, no. 4, pp. 28–39,Aug. 2002.
[2] M. Bhardwaj, R. Min, and A. Chandrakasan, "Quantifying and enhancing power awareness of VLSI systems," IEEE Trans. Very Large ScaleIntegr. (VLSI) Syst., vol. 9, no. 6, pp. 757–772, Dec. 2001.
[3] A. Wang and A. Chandrakasan, "Energy-aware architectures for a realvalued FFT implementation," in Proc. IEEE Int. Symp. Low PowerElectron. Design, Aug. 2003, pp. 360–365.
[4] T. Kuroda, "Low power CMOS digital design for multimedia processors," inProc. Int. Conf. VLSI CAD, Oct. 1999, pp. 359–367.
[5] H. Lee, "A power-aware scalable pipelined booth multiplier," in Proc.IEEE Int. SOC Conf., Sep. 2004, pp. 123–126.
[6] S.-R. Kuang and J.-P. Wang, "Design of power-efficient configurablebooth multiplier," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57,no. 3, pp. 568–580, Mar. 2010.
[7] O. A. Pfander, R. Hacker, and H.-J. Pfleiderer, "A multiplexer-based concept for reconfigurable multiplier arrays," inProc. Int. Conf. Field Program. Logic Appl., vol. 3203. Sep. 2004, pp. 938–942.
[8] F. Carbognani, F. Buergin, N. Felber, H. Kaeslin, and W. Fichtner,"Transmission gates combined with level-restoring CMOS gates reduce glitches in low-power low-frequency multipliers," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 7, pp. 830–836, Jul. 2008.
[9] T. Yamanaka and V. G. Moshnyaga, "Reducing multiplier energy by data-driven voltage variation," inProc. IEEE Int. Symp. Circuits Syst.,May 2004, pp. 285–288.
[10] W. Ling and Y. Savaria, "Variable-precision multiplier for equalizer with adaptive modulation," inProc. 47th Midwest Symp. Circuits Syst.,vol.1. Jul. 2004, pp. I-553–I-556.

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