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CASCADED MULTI LEVEL INVERTER BASED STATCOMUSING FUZZY LOGIC CONTROLLER FOR HIGH-POWER APPLICATIONS

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ABSTRACT-**In this paper, a simple static var compensatingscheme using a cascaded multilevel inverter-based STATCOM is proposed. The topology consists of two standard inverters are connected in cascade through open-end windings of athree-phase transformer. The dc-link voltages of the inverters areregulated at different levels to obtain multilevel operation. A fuzzy logic control scheme is proposed for the controlling operation of statcom. Thesimulation study is carried out in MATLAB/SIMULINK to predict the performance of the proposed scheme under balanced andunbalanced supply-voltage conditions. A laboratory prototype isdeveloped to validate the simulation results. The control schemeis implemented using the TMS320F28335 digital signal processor.Further, stability behavior of the topology is investigated. Thedynamic model is developed and transfer functions are derived.The system behavior is analyzed for various operating conditions.**

***Index Terms*—DC-link voltage balance, multilevel inverter, power quality (PQ), static compensator (STATCOM)..**

I. INTRODUCTION

Static VAR compensators control only one of the three important parameters (Voltage, impedence, phase angle) determining the power flow in the AC power systems viz. the amplitude of voltage at selected terminals of the transmission line. It has long been realized that an all solid-state or advanced, static VAR compensator, which is true equivalent of ideal synchronous condenser, is technically feasible with the use of gate turn-off (GTO) thyristors.

Theapplication of (FACTS) controllers, such flexible ac transmission systems as static compensator (STATCOM) and static synchronous series compensator (SSSC), is increasing in power systems. This is due to their ability to stabilize the transmission systems and to improve power quality (PQ) in distribution systems. STATCOM is popularly accepted as a reliable reactive power controller replacing conventional var compensators, such as the thyristor-switched capacitor (TSC) and thyristor-controlled reactor (TCR). This device provides reactive power compensation, active power oscillation damping, flicker attenuation, voltage regulation,etc. .

Generally, in high-power applications, var compensation is achieved using multilevel inverters [2]. These inverters consist of a large number of dc sources which are usually realized by capacitors. Hence, the converters draw a small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. Balancing these voltages is a major research challenge in multilevel inverters. Various control schemes using different topologies are reported in [3]–[7]. Among the three conventional multilevel inverter topologies,cascade H-bridge is the most popular for static var compensation [5], [6]. However, the aforementioned topology requires a large number of dc capacitors. The control of individual dc-link voltage of the capacitors is difficult.

Static var compensation by cascading conventional multilevel/two level inverters is an attractive solution for high-power applications. The topology consists of standard multilevel/three level inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drives [8]. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of the inverters, the number of levels in the output voltage waveform can be increased. This improves PQ [8]. Therefore, overall control is simple compared to conventional multilevel inverters.

Various var compensation schemes based on this topology are reported in [10]–[12]. In [10], a three-level inverter and twolevel inverter are connected on either side of the transformer low-voltage winding. The dc-link voltages are maintained by separate converters. In [11], three-level operation is obtained by using standard two-level inverters. The dc-link

voltage balance between the inverters is affected by the reactive power supplied to the grid.

In this paper, a static var compensation scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The topology uses standard two-level inverters to achieve multilevel operation. The dc-link voltages of the inverters are regulated at asymmetrical levels to obtain four-level operation. To verify the efficacy of the proposed control strategy, the simulation study is carried out for balanced and unbalanced supply-voltage conditions. A laboratory prototype is also developed to validate the simulation results.

From the detailed simulation and experimentation by the authors, it is found that the dc-link voltages of two inverters collapse for certain operating conditions when there is a sudden change in reference current. In order to investigate the behavior of the converter, the complete dynamic model of the system is developed from the equivalent circuit. The model is linearized and transfer functions are derived. Using the transfer functions, system behavior is analyzed for different operating conditions.

This paper is organized as follows: The proposed control scheme is presented in Section II. Stability analysis of the converter is discussed in Section III. Simulation and experimental results are presented in Sections IV and V, respectively.

II. Cascaded multi-Level Inverter-Based STATCOM

Fig. 1 shows the power system model considered in this paper [13]. Fig. 2 shows the circuit topology of the cascaded two-level inverter-based multilevel STATCOM using standard two-level inverters. The inverters are connected on the low-voltage (LV) side of the transformer and the high-voltage (HV) side is connected to the grid. The dc-link voltages of the inverters are maintained constant and modulation indices are controlled to achieve the required objective. The proposed control scheme is derived from the ac side of the equivalent circuit which is shown in Fig. 3. In the figure, v'_a, v'_b and v'_c are the source voltages referred to LV side of the transformer, r_a, r_b and r_c are the resistances which represent the losses in the transformer and three inverters, L_a,L_b and L_c are leakage inductances of transformer windings, and e_{a1}, e_{b1}, e_{c1} ,e_{a2}, e_{b2}, e_{c2} and e_{a3}, e_{b3}, e_{c3} are the output voltages of inverters 1,2 and 3, respectively. r_1,r_2,r_3 are the leakage resistances of dc-link capacitors c_1, c_2 and c_3 , respectively. Assuming $r_a = r_b = r_c =$ r, $L_a = L_b = L_c = L$ and applying KVL on the ac side, the dynamic model can be derived using [14] as

$$\begin{bmatrix} \frac{di'_a}{dt} \\ \frac{di'_b}{dt} \\ \frac{di'_c}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & 0 \\ 0 & \frac{-r}{L} & 0 \\ 0 & 0 & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i'_a \\ i'_b \\ i'_c \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v'_a - (e_{a1} - e_{a2}) \\ v'_b - (e_{b1} - e_{b2}) \\ v'_c - (e_{c1} - e_{c2}) \end{bmatrix} \quad (1)$$

Equation (1) represents the mathematical model of the cascaded two-level inverter-based multilevel STATCOM in the stationary reference frame. This model is transformed to the synchronously rotating reference frame [14]. The – axes reference voltage components of the converter and are controlled as

$$e^*_d = -x_1 + \omega L i'_q + v'_d \quad (2)$$

$$e^*_q = -x_2 + \omega L i'_d + v'_q \quad (3)$$

Where v'_d is the d-axis voltage component of the ac source and i'_d,i'_q are d,q- axes current components of the cascaded inverter, respectively. The synchronously rotating frame is aligned with source voltage vector so that the q-component of the source voltage v'_q is made zero. The control parameters and are controlled as follows:

$$x_1 = \left(k_{p1} + \frac{k_{i1}}{s}\right)(i^*_d - i'_d) \quad (4)$$

$$x_2 = \left(k_{p2} + \frac{k_{i2}}{s}\right)(i^*_q - i'_q) \quad (5)$$

The d-axis reference current i^*_d is obtained as

$$i^*_d = \left(k_{p3} + \frac{k_{i3}}{s}\right)[(v^*_{dc1} + v^*_{dc2}) - (v_{dc1} + v_{dc2})] \quad (6)$$

where v^*_{dc1}, v^*_{dc2}, v^*_{dc3} and v_{dc1}, v_{dc2}, v_{dc3} are the reference and actual dc-link voltages of inverters 1 and 2, respectively. The q-axis reference current i^*_q is obtained either from an outer voltage regulation loop when the converter is used in transmission-line voltage support [5] or from the load in case of load compensation [16].

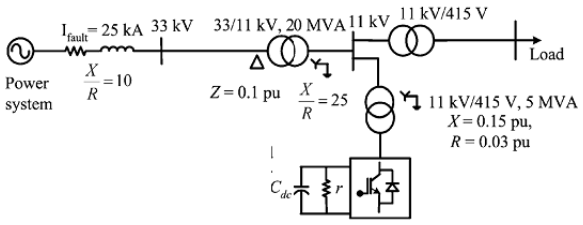


Fig. 1. Power system and the STATCOM model.

A .Control strategy

The control block diagram is shown in Fig. 4. The unit signals $\cos\omega t$ and $\sin\omega t$ are generated from the phase-locked loop (PLL) using three-phase supply voltages [14]. The converter currents are transformed to the synchronous rotating reference frame using the unit signals. The switching frequency ripple in the converter current components is eliminated using a low-pass filter (LPF). From $(v^*_{dc1} + v^*_{dc2})$ and i^*_qloops, the controller generates d–q axes reference voltages, $e^*_d$and e^*_q for the cascaded inverter. With these reference voltages, the inverter supplies the desired reactive current and draws required active

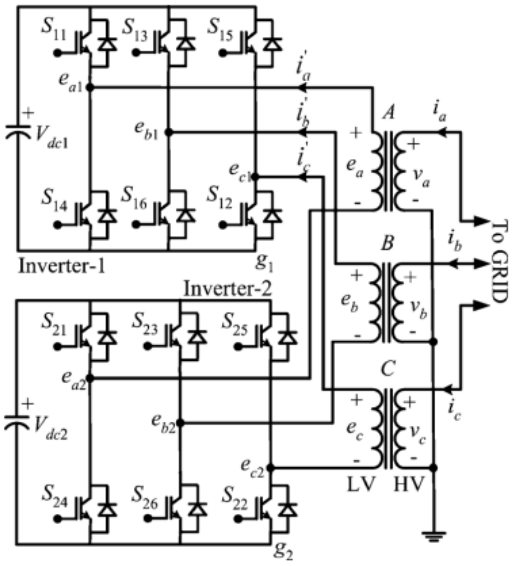


Fig. 2. Cascaded two-level inverter-based multilevel STATCOM.

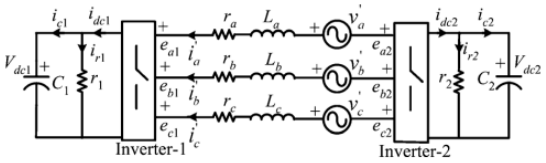


Fig. 3. Equivalent circuit of the cascaded two-level inverter-based multilevel STATCOM

current to regulate total dc-link voltage $(v^*_{dc1} + v^*_{dc2})$. However, this will not ensure that individual dc-link voltages are controlled at their respective reference values. Hence, additional control is required to regulate individual dc-link voltages of the inverters.

B . DC link balance controller:

The resulting voltage of the cascaded converter can be given as $e_I\angle\delta$, where $e_I = \sqrt{e_d^2 + e_q^2}$ and $\delta = \tan^{-1}\left(\frac{e_q}{e_d}\right)$. The active power transfer between the

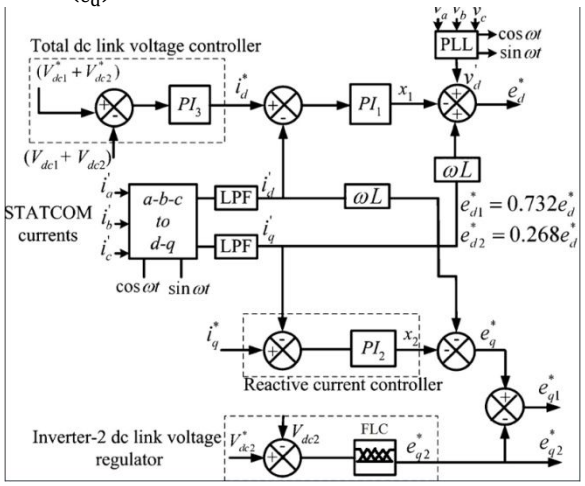


Fig. 4. Control block diagram

source and inverter depends on δand is usually small in the inverters supplying var to the grid [1]. Hence, δcan be assumed to be proportional toe_q.Therefore, the q-axis reference voltage component of inverter-2$e^*_{q2}$is derived from the fuzzy logic controller to control the dc-link voltage of inverter-2

The fuzzy logic toolbox is highly impressive in all respects. It makes fuzzy logic an effective tool for the conception and design of intelligent systems. The fuzzy logic toolbox is easy to master and convenient to use. And last, but not least important, it provides a reader friendly and up-to-date introduction to methodology of fuzzy logic and its wide ranging applications.

Fuzzy inference is a method that interprets the values in the input vector and, based on user defined rules, assigns values to the output vector. Using the GUI editors and viewers in the Fuzzy Logic Toolbox, you can build the rules set, define the membership functions, and analyze the behavior of a fuzzy inference system (FIS). The following editors and viewers are provided.

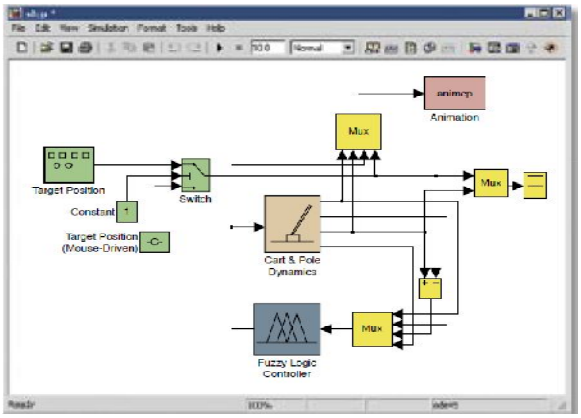


Fig.4(a).fuzzy inference system

The q-axis reference voltage component of inverter-1 e^*_{q1} is obtained as

$$e^*_{q1} = e^*_q - e^*_{q2} \quad (7)$$

The dc-link voltage of inverter-2 is controlled at 0.366 times the dc-link voltage of inverter-1 [9]. It results in four-level operation in the output voltage and improves the harmonic spectrum. Expressing dc-link voltages of inverter-1 and inverter-2 in terms of total dc-link voltage, V_{dc} as

$$V_{dc1}=0.732V_{dc} \quad (8)$$

$$V_{dc2}=0.268V_{dc} \quad (9)$$

Since the dc-link voltages of the two inverters are regulated, the reference d-axis voltage component e^*_d is divided in between the two inverters in proportion to their respective dc-link voltage as

$$e^*_{d1}=0.732e^*_d \quad (10)$$

$$e^*_{d2}=0.268e^*_d \quad (11)$$

For a given power, if $V_{dc2} < v^*_{dc2}$, $\delta_2 \left(\tan^{-1}\left(\frac{e^*_{q2}}{e^*_{d2}}\right)\right)$ increases and $\delta_1 (= \tan^{-1}(\frac{e^*_{q1}}{e^*_{d1}}))$ decreases. Therefore, power transfer to inverter-2 increases, while it decreases for inverter-1. The power transfer to inverter-2 is directly controlled, while for inverter-1, it is controlled indirectly. Therefore, during disturbances, the dc-link voltage of inverter-2 is restored to its reference quickly compared to that of inverter-1. Using e^*_{d1} and e^*_{q1}, the reference voltages are generated in stationary reference frame for inverter-1 and using e^*_{d2} and e^*_{q2} for inverter-2. The reference voltages generated for inverter-2 are in phase opposition to that of inverter-1. From the reference voltages, gate signals aregenerated using the sinusoidal pulse-width modulation (PWM) technique [15]. Since the two inverters' reference voltages are in phase opposition, the predominant harmonic appears at double the switching frequency.

C .unbalanced conditions:

Network voltages are unbalanced due to asymmetric faults or unbalanced loads [16]. As a result, negative-sequence voltage appears in the supply voltage. This causes a double supply frequency component in the dc-link voltage of the inverter. This double frequency component injects the third harmonic component in the ac side [17]. Moreover, due to negative-sequence voltage, large negative-sequence current flows through the inverter which may cause the STATCOM to trip [16]. Therefore, during unbalance, the inverter voltages are controlled in such a way that either negative-sequence current flowing into the inverter is eliminated or reduces the unbalance in the grid voltage. In the latter case, STATCOM needs to supply large currents since the interfacing impedance is small. This may lead to tripping of the converter.

The negative-sequence reference voltage components of the inverter e^*_{dn} and e^*_{qn} are controlled similar to positive-sequence components in the negative synchronous rotating frame as [18]

$$e^*_{dn} = -x_3 + (-\omega L)i'_{qn} + v'_{dn} \quad (12)$$

$$e^*_{qn} = -x_4 - (-\omega L)i'_{dn} + v'_{qn} \quad (13)$$

Where v'_{dn}, v'_{qn} are - axes negative-sequence voltage components of the supply i'_{dn} and i'_{qn} are d-q axes negative-sequence current components of the inverter, respectively. The control parameters and are controlled as follows:

$$x_3 = \left(k_{p5} + \frac{k_{i5}}{s}\right)(i^*_{dn} - i'_{dn}) \quad (14)$$

$$x_4 = \left(k_{p6} + \frac{k_{i6}}{s}\right)(i^*_{qn} - i'_{qn}) \quad (15)$$

The reference values for negative-sequence current components i^*_{dn} and i^*_{qn} are set at zero to block negative-sequence current from flowing through the inverter.

III. Stability Analysis

Considering the dc side of the two inverters in Fig. 3, the
complete dynamics of the system are derived in the

Appendix.

The transfer function $\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)}$ is as follows:

$$\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)} = \frac{num_1(s)}{den(s)} \quad (16)$$

and the transfer function $\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)}$ is

$$\frac{\Delta\widehat{V_{dc2}}(s)}{\Delta\widehat{\delta_2}(s)} = \frac{num_2(s)}{den(s)} \quad (17)$$

Where $num_1(s), den(s)$ and $num_2(s)$ are given in the Appendix.

From the transfer functions (16) and (17), it can be observed that the denominator is a function of resistances ,reactances and modulation indices and $\sin 2_{(\delta_{10}-\delta_{20})}$. Although the denominator includes an operating condition term $(\delta_{10} - \delta_{20})$, the product $\sin 2_{(\delta_{10}-\delta_{20})}$ is always positive. Hence, the poles of transfer function always lie on the left half of the s-plane. However, numerators of the transfer functions are functions of the operating conditions of$i'_{d0} i'_{q0}, \delta_{10}$and δ_{20}. The positions of zeros primarily depend on i'_{q0}, δ_1 and δ_2. The sign of these variables changes according to the mode of operation. Therefore, zeros of thetransfer functions shift to the right half of the -plane for certain operating conditions. This system is said to be non minimumphase and there is a limit on *achievable dynamic response* [19]. The system may exhibit oscillatory instability when there is a step change in reference for high controller gains. Therefore, the controller gains should be designed suitably to avoid the instability. This behavior is similar to that of the two-level inverter-based STATCOM [20], [21].

The transfer function $\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)}$ for i'_{q0} =1.02 p.u., (capacitive mode) is given in (19), shown at the bottom of the page. From (19), it can be observed that all poles as well as all zeros lie on the left half of the s-plane for this operating condition. Fig. 5 shows the frequency response of the transfer function $\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)}$ for the same operating condition. From the figure, it can be observed that the system has sufficient gain and phase margins for this operating condition. Fig. 6 shows an enlarged root locus of the transfer function $\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)}$ when STATCOM is in inductive mode of operation. The reactive component i'_{q0} is set at 0.75 p.u. and proportional gain is varied from 0 to 10. It can be seen that all poles lie on the left half of the -plane for this case as well. However, one zero shift to the right half and three zeros lie on the left half of the s-plane. Moreover, it can be seen that closed-loop poles of the system shift to the right half of the s-plane for high controller gains.

IV. Simulation Results

The system con figuration shown in Fig. 1 is considered for simulation. The simulation study is carried out using MATLAB/ SIMULINK. The system parameters are given in Table I.

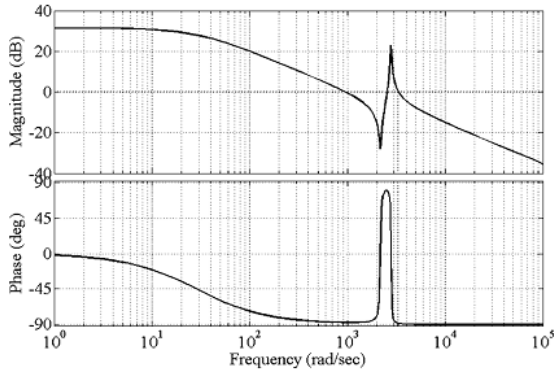


Fig.5. Frequency response $\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)}$ at i'_{q0} =1.02 p.u., $\delta_1 = -0.9^0, \delta_2 = 178.9^0 R_1$ =80 p.u., R_2 =60 p.u.

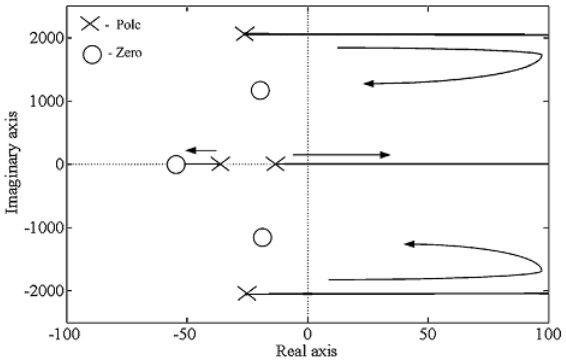


Fig.6. Frequency response $\frac{\Delta\widehat{V_{dc1}}(s)}{\Delta\widehat{\delta_1}(s)}$ at $i'_{q0} = -0.75$ p.u., $\delta_1 = 0.57^0, \delta_2 = -179.6^0 R_1$ =80 p.u., R_2 =60 p.u.

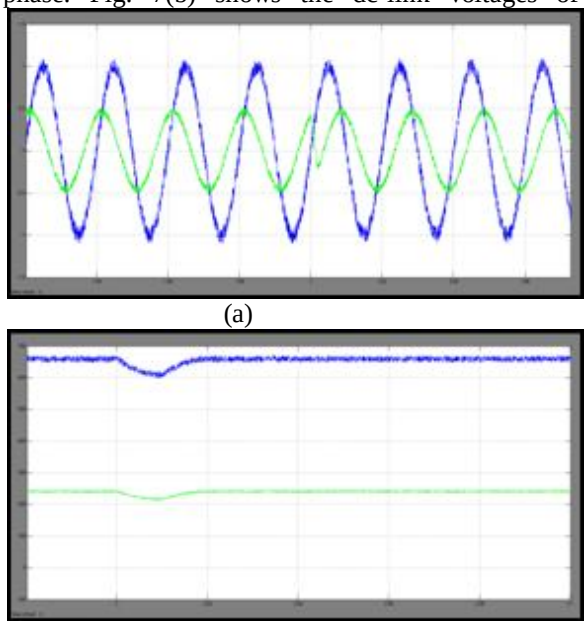
$$\frac{(s + 17.7)(s + 35.1 + j2170.6)(s + 35.1 - j2170.6)}{(s + 15.4)(s + 32.4 + j2786.6)(s + 24.2 - j2786.6)} \quad (18)$$

TABLE-I
SIMULATION SYSTEM PARAMETERS

Rated Power	5MVA
Transformer voltage rating	11kv/400
AC supply frequency, f	50Hz
Inverter-1 dc link voltage, V_{dc1}	659v
Inverter-1 dc link voltage, V_{dc2}	241v
Transformer leakage reactance, X_l	15%
Transformer resistance, R	3%
DC link capacitances, C_1,C_2	50mF
Switching frequency	1200Hz

A. Reactive Power Control

In this case, reactive power is directly injected into the grid by setting the reference reactive current i_q^*component at a particular value. Initially,i_q^* is set at 0.5 p.u. At t=2.0 s,i_q^* is changed to 0.5 p.u. Fig. 7(a) shows the source voltage and converter current of the phase. Fig. 7(b) shows the dc-link voltages of

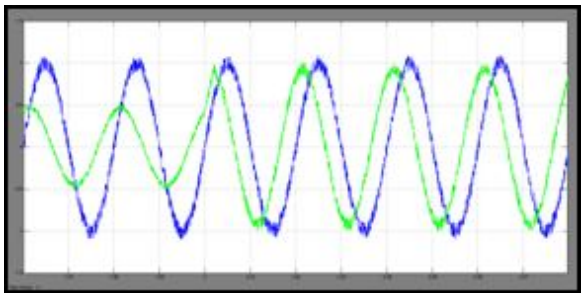


(a)

(b)

Fig. 7. Reactive power control. (a) Source voltage and inverter current. (b) DC-link voltages of two inverters.

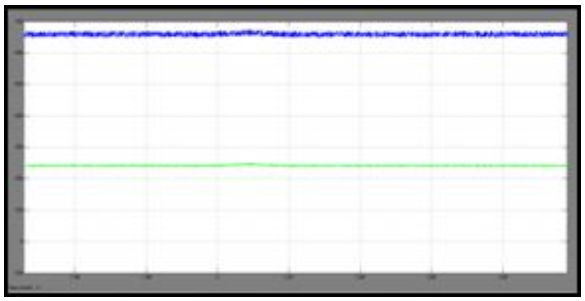
two inverters. From the figure, it can be seen that the dc-link voltages of the inverters are regulated at their respective reference values when the STATCOM mode is changed from capacitive to inductive. Moreover, the dc-link voltage of inverter 2 attains its reference value faster compared to that of inverter 1 as discussed in Section II.



(a)

B.Load Compensation:

In this case, the STATCOM compensates the reactive power of the load. Initially, STATCOM is supplying a current of 0.5 p.u. At t=2.0 s, the load current is increased so that STATCOM supplies its rated current of 1 p.u. Fig. 8(a) shows source voltage and converter current, while Fig. 8(b) shows the dc-link voltages of two inverters. The dc-link voltages are maintained at their respective reference values when the operating conditions are changed.



(b)

Fig. 8. Load compensation. (a) Source voltage and inverter current. (b) DC-link voltages of two inverters.

C . Operation during fault condition:

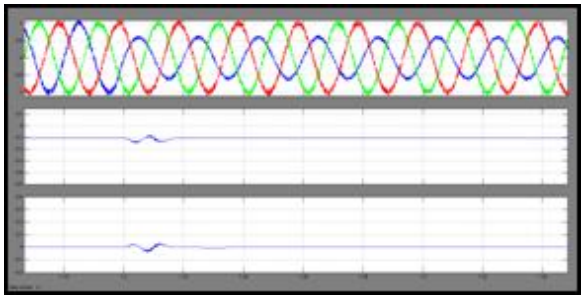


Fig. 9. Operation During Fault. (A) Grid Voltages OnThe Lv Side Of The Transformer. (B) D-Axis Negative-Sequence Current Component $i_{dn}^{'}$.(C) Q Axis Negative-Sequence Current Component $i_{qn}^{'}$.

In this case, a single-phase-to-ground fault is created at t=1.2 s, on the phase of the HV side of the 33/11-kV transformer. The fault is cleared after 200 ms. Fig. 9(a) shows voltages across the LV side of the 33/11-kV transformer. Fig. 9(b) and (c) shows the d-q axes components of negative-sequence current of the converter. These currents are regulated at zero during the fault condition.

VI. CONCLUSION

DC-link voltage balance is one of the major issues in cascaded inverter-based STATCOMs. In this paper, a simple var compensating scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The scheme ensures regulation of dc-link voltages of inverters at asymmetrical levels and reactive power compensation. The performance of the scheme is validated by simulation and experimentations under balanced and unbalanced voltage conditions. Further, the cause for instability when there is a change in reference current is investigated. The dynamic model is developed and transfer functions are derived. System behavior is analyzed for various operating conditions. From the analysis, it is inferred that the system is a non minimum phase type, that is, poles of the transfer function always lie on the left half of the s-plane. However, zeros shift to the right half of the s-plane for certain operating conditions. For such a system, oscillatory instability for high controller gains exists.

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