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AN OPTIMIZED IMPLEMENTATION OF 16-BIT MAGNITUDE COMPARATOR CIRCUIT USING DIFFERENT LOGIC STYLE OF FULL ADDER

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Abstract:

In VLSI applications, area, delay and power are the important factors which must be taken into account in the design of a fast adder [1]. The paper attempts to examine the features of certain adder circuits which promise superior performance compared to existing circuits. The advantages of these circuits are low-power consumption, a high degree of regularity and simplicity. In this paper, the design of a 16-bit comparator is proposed. Magnitude comparison is one of the basic functions used for sorting in microprocessor, digital signal processing, so a high performance, effective magnitude comparator is required. The main objective of this paper is to provide new low power, area solution for Very Large Scale Integration (VLSI) designers using low power high performance efficient full adders.

Keywords— X greater than Y(XgY),X less than Y(XlY),X equal to Y(XeY) ,Power delay product (PDP),LowPower(LP), High-Performance (HP), FA24T, N-10T,Bridge.

I. Introduction

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number. So comparator is used for this purpose. The comparator is a very basic and useful arithmetic component of digital systems that compares the magnitude of two binary numbers and determines if the numbers are equal, or if one number is greater than or less than the other number. One can implement the comparator by flattening the logic function directly Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes (Fig.1.1). The outcome of comparison is specified by three binary variables that indicate whether A>B, A=B, or A<B.

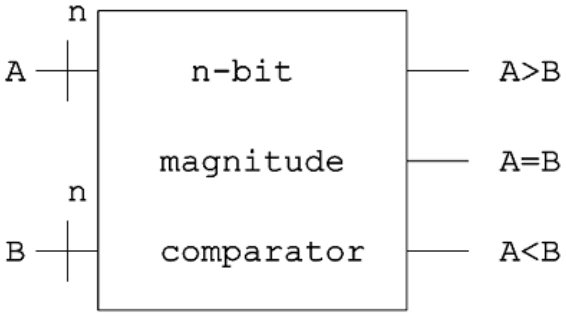

Figure 1.1: block diagram of n-bit magnitude comparator

The circuit, for comparing two n-Bit numbers, has 2n inputs & 2 2n entries in the truth table, for 1-Bit numbers, 2-inputs & 4-rows in the truth table, similarly, for 2-Bit numbers 4-inputs & 16-rows in the truth table. The logic style used in logic

gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and on the wiring complexity.

The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance.

A compact, good cost benefit, high-performance ratio comparator plays an important role in almost all hardware sorters.

II. EFFICIENT FULL ADDER:

Some of the standard efficient full adders are compared and the full adder with less power is considered for the design of RCA and three stages of CSA.

2.1 REVIEW OF THREE STATE-OF- ART FULL ADDER CELLS

There are different types of CMOS full adder. This section reviewed the three state-of-the-art 1-bit full adders. This proposed cell is compared with them.

The Bridge circuit has 26 transistors this design creates a conditional conjunction between two circuit nodes. Full Adders which are based on fully symmetric CMOS style are called Bridge Full Adders.

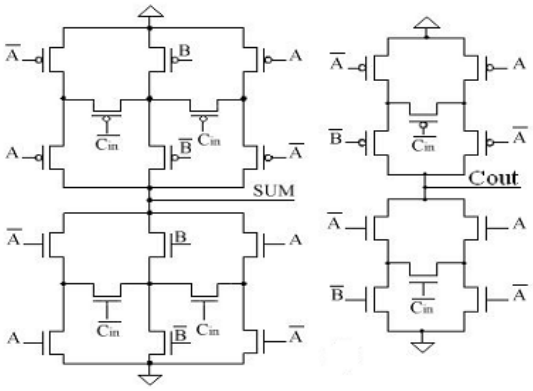

Figure 2.1: Bridge Full Adder

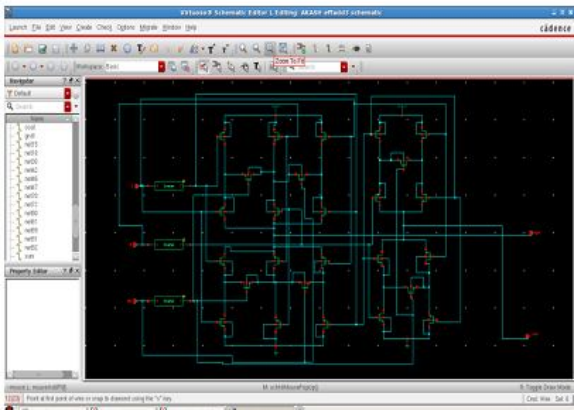

Figure 1.2: Schematic of bridge Full Adder

The full-adder with 24 transistors (FA24T) has 24 transistors this full Adder is based on Bridge style. The body of FA24T has two transistors less than Bridge and has better power consumption. In FA24t, a bridge circuit generates Cout and another bridge circuit is utilized in series with the prior to generate sum.

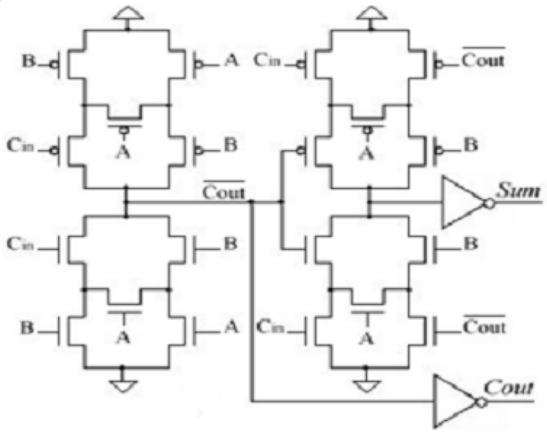

Figure 2.2: FA24T Full Adder

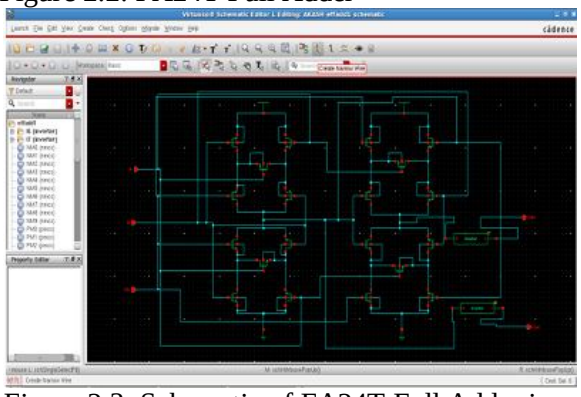

Figure 2.3: Schematic of FA24T Full Adder in cadence tool

III. RELATED RESEARCH WORKS

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates. The logic for sum requires XOR gate while the logic for carry requires AND, OR gates.

The XOR gate is the basic building block of the full adder circuit. The performance of the full adder can be improved by enhancing the performance of the XOR gate. Several refinements have been made in its structure in terms of transistors to increase the performance of full adder. The early designs of XOR gates were based on eight transistors or six transistors that are conventionally used in most designs. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip. There by reducing the area and delay. There by educing the area and delay. reducing the area and delay.

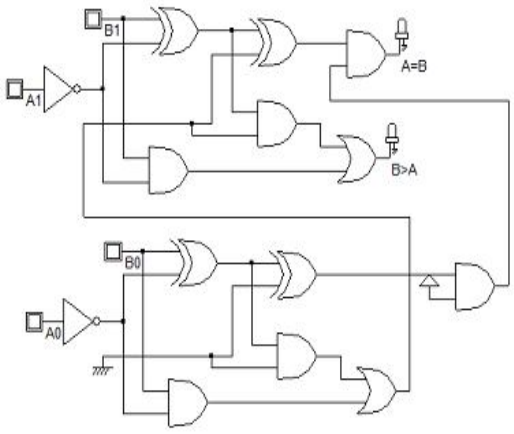

Fig.3.Logic diagram of basic full adder comparator

The layout design of the basic full adder based comparator is shown in fig.4... layout is the general concept that describes the geometrical representation of the circuits by the means of layers.Different logical layers is used by designers to generate the layout.

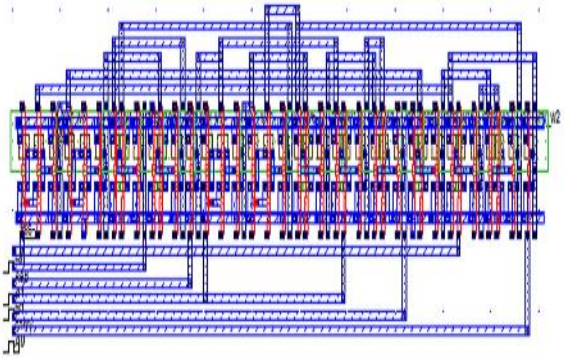

Fig.4.layout design of basic full adder based comparator

IV. PROPOSED WORK

Proposed work of comparator is based on another logic style of full adder.thislogic style of comparator provides less power consumption than other logic styles described in this paper.

The implementation of new logic full adder based comparator is shown in fig.9.It consists of two full adders, two not gates at one of the input and two AND gates at the output of the comparator.

It has four input (A1, B1, A0, B0) and two output (A=B, B>A).

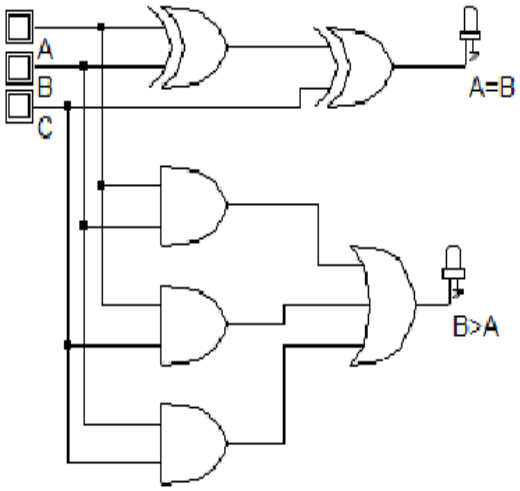

Fig.5.logic diagram of full adder using logic

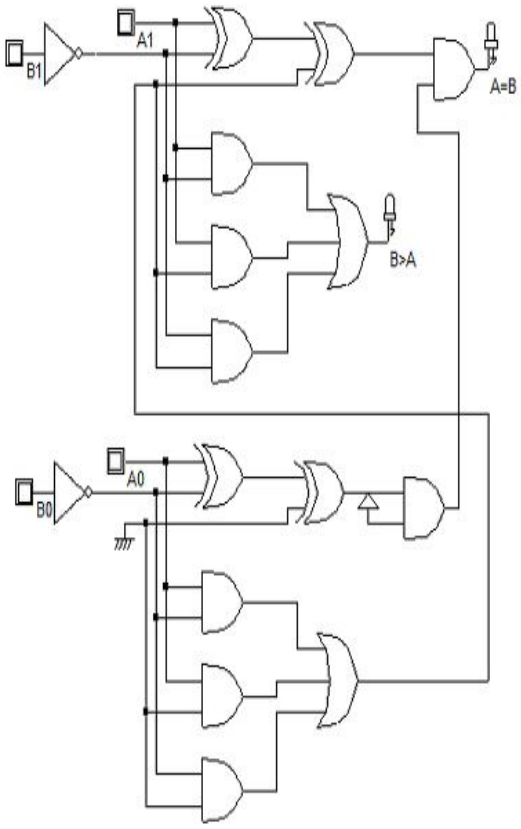

Fig.6 logic diagram of proposed full adder based comparator

The layout design of comparator using another logic of full adder is shown in fig.10.layout is the general concept that describes the geometrical representation of the circuits by the means of layers and polygons. Different logical layers are used by designers to generate the layout. Different logical layers are used by the designers to generate the layout.

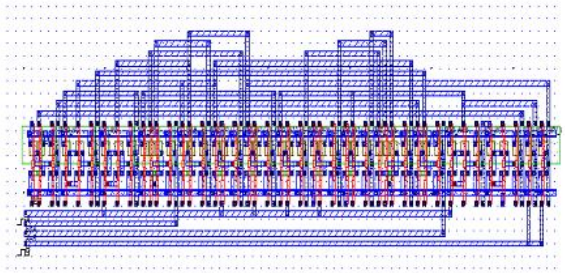

Fig.10.layout design of proposed full adder based comparator

ANALYSIS AND RESULT

When we started, implementation of 4-bit magnitude comparator in BDD, then the total product terms was 78 that means 78 node count , but with the help of BDD package tool it reduced to 46 node count. Now one node is represented by a 2x1 multiplexer. After synthesizing 2x1 multiplexer in Synopsys tool, the power required for it is 762.3125 nw. Since we have total 46 nodes so total power taken by 4-bit comparator is 46*762.3125 nw which is equal to 35.0664 µw. When we synthesized 4-bit magnitude comparator in Synopsys tool then the power comes as 164.29 µw.After applying pre-computation technique in comparator then the total power comes as 66.6735 µw which is less then compare to without applying pre-computation technique in comparator. But when we compare all the three ways then we can conclude that, implementation of 4-bit magnitude comparator through BDD is the best way for low power aspect.

COMPARISON

	BDD	Synopsys	Pre-computation
Power	35.0664 µw	164.29 µw	66.6735 µw

V. CONCLUSION AND FUTUREWORK

With power and area being a limiting factor in high density and high-performance VLSI designs, a great deal of effort has been made to explore low-power and area design options without sacrificing performance. After simulation of all four designs final results are obtained for Power Consumption, Delay, Power Delay Product. PTL Logic Style provides low power design as compared to CMOS Logic Style. PTL Logic Style provides less PDP as compared to CMOS logic style. It has been found that transistor count is less in PTL style design than that of CMOS logic style design. An important factor, output voltage swing is better in CMOS logic style design & Transmission Gate design. But Transmission Gate logic style requires transistor count more than CMOS design style.PTL style do not provide full output voltage swing. Power, delay and PDP for low power comparator is less than the conventional comparator. In future the design of comparator will take less number of transistors than the existing one with low power and high PDP value. The comparisons of comparator

design are based upon BSIM3V3 250nm technology in tanner EDA tool.

REFERENCES

[1] S.Chaudhury and S.Chattopadhyay "Output phase assignment for area and power optimization in multi-level multi-output combinational logic circuits".

[2] B. Yang. "Optimizing Model Checking based on BDD Characterization." School of Computer Science –Carnegie Mellon University, May 1999. Available as researchreport CMU-CS-99-129.

[3] S. B. Akers, "Binary Decision Diagram," IEEE Trans. Computers, Vol. 27, 1978.

[4] K. S. Brace and R. L. Rudell and R. E. Bryant, "Efficient Implementation of a BDD Package," Design Automation Conference, 1990.

[5] P.W.C. Prasad, and A. K. Singh, "AnEfficient Method for Minimization of Binary Decision Diagrams," 3rd International Conference on Advances in Strategic Technologies (ICAST), pp. 683-688, 2003.

[6] MazharAlidina, Jose Monteiro, SrinivasDevadas, "Pre-computation based sequential logic optimization for low power", IEEE transaction on VLSI system, No.4 , DECEMBER 1994.

[7] ONDREJ LHOTAK and LAURIE HENDREN, " Evaluating the Benefits of Context-Sensitive Pointsto Analysis Using a BDD-Based Implementation" Sep 2008, ACM, Proceedings of the 15thInternational Conference on Compiler Construction. (page 19)

[8] Robert Wille and Rolf Drechsler, "BDD based synthesis of reversible logic for large function", Design automation conference,2009, DAC'09.46thACM/IEEE.

[9] Fei Sun and Yinshui Xia, "BDD based detection algorithm for xor-type logic", 2008 11thIEEE international conference on communication technology proceedings .

[10] M.Morris Mano "digital logic and computer design" PRENTICE-HALL, INC., ENGLEWOOD CLIFFS, 2009

[11] A. Anand Kumar "Fundamentals of Digital Design circuits", 2ndedition, PHI Learning private limited-2009

[12] Nagayama, S., A. Mishchenko, T. Sasao and J.T. Butler, 2003. "Minimization of average path length in BDDs by variable reordering".Intl. Workshop on Logic and Synthesis.

[13] A. Raghunathan and N. Jha " Behavioral synthesis for low power." In Proceedings of the International Conference on Computer Design, pages 318–322, Boston, MA, Oct. 1994.

[14] Chandrakasan, A.P., and Brodersen, R.W., "Low Power Digital CMOS Design," Kluwer Academic Publishers, 1995.

[15] R. Rudell, "Dynamic variable ordering for ordered binary decision diagrams," International Conference on Computer-Aided Desing, pp. 42–47, 1993.

[16] Shih-Chieh Chang, David Ihsin Cheng and MalgorzataMarek-Sadowska, "Minimizing ROBDD size of incompletely specified multiple output function", European Design and Test Conference, 1994.