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Voltage Balance Control and stability for the load by using a Multi winding High-Frequency Transformer

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***Abstract*—In this paper, a novel modular cascaded multi-level converter with multiwinding high-frequency (MWHF) trans-former is proposed for medium- or high-voltage applications. In the proposed converter, a cascaded *H* -bridge rectifier (CHBR) is connected directly with the input ac source while the traditional step-down transformer is no longer necessary. Then, an isolated dc–dc converter composed by a group of *H* -bridge converters and a MWHF transformer with high power density is used to isolate the dc buses produced by the CHBR. The equivalent circuit and mathematical model of the MWHF transformer and the high frequency (HF) converter are obtained firstly in this paper. Then, the voltage stability under unbalanced loads is analyzed and the naturally balance ability is verified. To accelerate the dc bus voltage balancing process, a voltage balance control based on energy exchange between different transformer windings is proposed that is realized by accomplishing the phase shift adjustment of the terminal voltages on different windings. Simulations and experiments are implemented to verify the performance of the proposed converter.**

***Index Terms*—*H*-bridge, high-frequency (HF) transformer,multilevel converter, voltage balance control.**

I. INTRODUCTION

Multilevel converters gain an increasing attention on medium- and high-voltage applications because of thevoltage limitations on unit power electronic devices. To simplify the control and improve the reliability, many kinds of multilevel topologies are proposed. The first kind is neutral-point-clamped (NPC) converters where a lot of clamping diodes or capacitors are needed to balance the neutral point voltage, and the number of clamping diodes and capacitors will increase significantly along with the increase of voltage levels [1]. Another kind is cascaded *H* -bridge converter that is modular and the clamping devices are unnecessary. But an industrial-frequency multiwinding isolated transformer is needed to produce the isolated and balanced voltage for the cascaded modules. The transformer also increases the cost and volume of the whole converter [2]. Some novel converter topologies are studied to reduce the system cost and volume, to increase the power density, and also to increase the stability by modular design. The modular designcan also simplify the converter structure and increase the fault operation capacity [3]–[5]. In [6]–[9], a transformer-less multi-level converter is proposed whose outputs in each module are not isolated. In this case, the output can only be connected with loads of multiphase motors or separate motors. The dc volt-ages are difficult to be balanced while the loads are unbalanced. In [10]–[17],

the medium or high-frequency (HF) transformer is used to realize isolation in the converters. The transformer working on higher frequency is of high power density com-pared to the industrial-frequency transformer. The methods for the control and reducing switching loss in theconverter with HF transformer have been studied in [18]. The converter proposed in [10] needs a high-voltage ac–ac converter that is difficult to be realized. The converter topology proposed by Akagi attracted a lot of researches, which is modular since the *H* -bridges are used for both the high-voltage rectifier and HF converters [13]. In the topology proposed in [13], the load unbalance will worsen the voltage balancing of the converters. So it can only feed balanced loads or can be cascaded again to feed one load. Otherwise, the dc bus on the secondary side must be connected in paral-lel to keep voltage balance when feeding isolated unbalanced loads [14]. The converters with HF transformer have also been studied for the applications in tractions that need higher power density [19]–[26]. A lot of researches have been implemented for the voltage balance control and the modulation methods for the HF converters [27]–[30]. In [32]–[35], the multiwinding transformer is used for the isolation and energy balance. The windings linking the same flux can realize energy exchange, which can be used to balance the load energy. So the voltage equalization can be realized easier.

In this paper, a novel modular multilevel converter is proposed where a multiwinding high-frequency (MWHF) transformer is used for the isolation and voltage balance. The cascaded *H* -bridge rectifier (CHBR) can be connected directly with theinput ac voltage without need of the step-down transformer. By modular and redundant design, the converter is with high reliability and capable of fault operation. Because all windings are

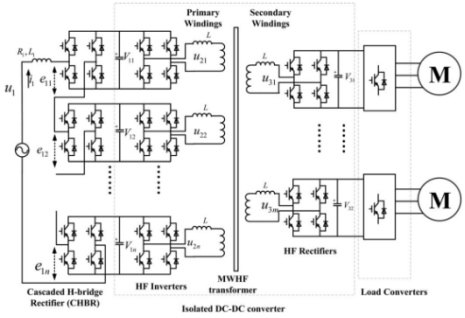


Fig. 1.Topology of the proposed converter.

linked by the same flux inside the transformer, power can be transferred between the windings that merits in balancing the dc bus voltages under unbalanced loads. The self-balancing ability is analyzed in this paper. Furthermore, a voltage equalization method is proposed to enhance the dynamic performance of the voltage balance by the power control between the windings of the transformer. Since the dc buses on the secondary side of the transformer are all isolated, these dc buses and the load con-verters can be connected in series or in parallel just according to the applications [36]. Then, the loads with different power and voltage can be driven while the stability and balance of the converter can be maintained. Simulations and experiments are implemented to verify thestability of the proposed converter and the performance of the proposed control method.

II. TOPOLOGY OF THE CONVERTER

The proposed converter is shown in Fig. 1. There are three parts: the first is a cascaded *H* -bridge rectifier (CHBR) which is used to convert the input ac voltage to the cascaded dc buses. Because of the little limitation on cascaded levels, the CHBR can be connected with the grid voltage directly without using of step-down transformer. The second part is an isolated dc–dc converter with an MWHF transformer, which is of higher power density than an industrial-frequency transformer. A group of *H* -bridge converters together with the transformer windings are used to convert the dc voltages to HF ac voltages, or convert the HF ac voltages to dc voltages. To be convenient, the HF converters connected with the primary windings of the transformer are named as the HF inverters while the ones connected with the secondary windings are named as the HF rectifiers. The third part is load converters to feed all kinds loads with different voltages and powers (see Fig. 2).

To obtain clear description of the state variables, subscripts 11 to 1*n* mark the variables of CHBR, subscripts 21 to 2*n* mark HF inverters, and subscripts 31 to 3*m* mark HF rectifiers. *n* is the number of the primary windings while *m* is the number of the secondary windings. Variables u_1 and i_1 are the input voltage and current of the ac grid. L_1 and R_1 are the inductance and resistance series connected between the CHBR and the ac grid. Variable e_1 is the total output voltage of the CHBR while $e_{1\,1}$~ $e_{1n}$are the voltages outputting by *H* -bridge cells of theCHBR, while $e_1 = e_{1j}$. Variables e_{21}−e_{2n} are the back electromotive forces (EMFs) of the primary windings while $e_{31} - e_{3m}$are the back EMFs of the secondary windings. V_{11} −V_{1n} are the output dc bus voltages of the CHBR. V_{31}−V_{3m} are dc bus voltages output by the HF rectifiers. Variables u_{21}−$u_{2n}$are the

terminal voltages of the HF inverters. Variables $u_{31} - u_{3m}$ are the terminal voltages of the HF rectifiers.

In the proposed converter, the number of cascaded modules in CHBR is determined by the grid voltage and the voltage ratings of the semiconductor devices. The number of primary windings of the transformer is the same as the cascaded numbers in CHBR. Also some redundant modules can be added in the CHBR to increase the reliability. The number of the secondary windings can be designed flexibly according to the requirement of the loads. The voltage ratio of the transformer windings is designed as 1:1, so the *H* -bridge modules inside the CHBR and the HF converters can be interchangeable. Because all dc buses for the load converters are isolated by the transformer, the load converter can also be cascaded to enhance the output voltages, or be parallel connected to enhance the output current.

Compared with the traditional multilevel converters, the energy conversion in the proposed converter is completed through four high-frequency hard-switching stages.

Switching loss and conduction loss will decrease the efficiency of the whole converter. The loss can be reduced by using the MOSFET and SiC devices with low conduction and switching losses. The switching loss can also be reduced by some soft-switching technique as shown in [18], but it will increase the complexity of the circuit. In [19], the similar topology with four high-frequency hard-switching stages is applied on practical locomotive. The experimental results show that the efficiency of the converter is 96% with 8 cells cascaded. It also shows that as the increase of the cells cascaded, the efficiency will be decreased.

III. CONTROL OF THE CHBR

In the proposed converter, the cascade *H* -bridge rectifier (CHBR) is directly connected to the grid to produce separated dc buses. The control target of the CHBR is to keep the summarized dc bus voltages stable and to keep unity input power factor. The voltage balance between different dc buses is controlled by the isolated dc–dc converter and will be analyzed later in this paper. The output voltage of each *H* -bridge cell in CHBR is as follows (see Fig. 2):

$$e1_j = S1_j . V1_j \qquad (1)$$

where S_{1j} is the modulation factor of the *j*th cell of the CHBR, V_{1j} is the dc bus voltage of the *j*th cell, then

$$-1 \le S1_j \le 1 \qquad (2)$$

The output ac voltage of the whole CHBR is

$$e_1 = \sum_{j=1}^{n} e1_j = \sum_{j=1}^{n} (S1_j . V1_j) \qquad (3)$$

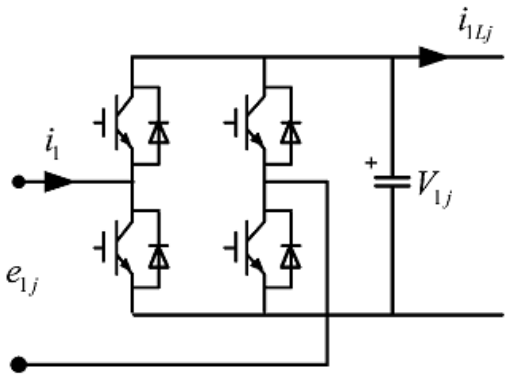


Fig. 2. Energy flows in one of the cells of *H* -bridge rectifier.

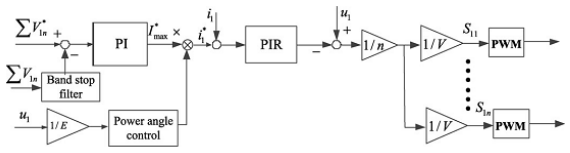


Fig. 3. Control strategy of the *H*-bridge rectifier.

The equation of the input voltage and current satisfy

$$L_1 \frac{di_1}{dt} + R_1 . i_1 = u_1 - e_1 \qquad (4)$$

The instant input power of the *j*th rectifier cell from the ac grid is

$$P_{1j} = e_{1j} . i_1 \qquad (5)$$

The energy stored in the capacitor is $(1/2)C1jV12j$, where $C1j$ is the capacitor of the dc bus. By the energy balance principle, the dynamic equation of the energy stored in the capacitors is

$$\frac{1}{2} C_{1j} \frac{dV_{1j}^2}{dt} = e_{1j} . i_1 - V1_j i_{1Lj} \qquad (6)$$

where $i1Lj$ is the load current on the dc bus of the *j*th cell. Assuming all dc bus capacitors are the same: $C11 = C12$

· · · = $C1n$ = $C1$, the energy stored in the capacitors of all cells can be expressed as

$$\frac{1}{2}C_1\frac{d\Sigma V_{1j}^2}{dt} = e_1.i_1 - \sum(V1_j i_{1Lj}) \quad (7)$$

By (1) and (5), (7) can be rewritten as

$$\frac{1}{2}C_1\frac{d\Sigma V_{1j}^2}{dt} = u_1.i_1 - R_1.i_1^2 - L_1.i_1\frac{di_1}{dt} - \sum(V1_j i_{1Lj}) \quad (8)$$

Assuming the load current as the disturbance, neglecting the effects of the resistance and inductance, the summarized voltage of all dc bus capacitors are determined by the difference of input and output power. Since the grid voltage is unchangeable, the input power is only determined by the input current. According to (6), the input current can be controlled by the output voltage e_1 of the CHBR. The control system of the CHBR is shown in Fig. 3, which is similar to [7]. The output of the voltage loop is the amplitude of the reference input current, and phase of the current can be controlled the same with the grid CHBR, the dc bus voltages contain twice-frequency oscillations since the input is a single-phase ac source. Hence a band-stop filter is usually used at the feedback loop of the dc voltage to compensate the twice-frequency oscillations and obtain the filtered average voltage value. In the traditional three-phase pulsewidthmodulated (PWM) rectifiers, proportional–integral (PI) regulators in synchronous frame are usually adopted to achieve zero steady-state error of the current control. But in single-phase PWM rectifiers, the PI regulator in synchronous frame cannot be used any more since the $d-q$ variables are no more constant. In the station-ary frame, since the current is of the sinusoidal waveforms, PI controller may not obtain a satisfying performance. Usually a proportional–integral–resonant (PIR) controller is used to get a better tracking performance at a certain frequency [6], [7]

$$G_i^{PIR}(s) = K_p + \frac{K_I}{s} + \frac{2K_R s}{S^2 + {\omega_0}^2} \quad (9)$$

Compared to the traditional PI regulator, a resonant part is added. The added resonant part$Gres(s) = 2KRs/(s2 + \omega o2)$ has infinite gain at the resonant frequency $\omega o$and approximately zero gain at any other frequencies. This property makes it suitable to regulate the ac currents. In our system, the resonant frequency $\omega o$is selected as the grid frequency. The coefficients KP and KR can be designed as same as the design of traditional PI regulators. In fact, in the PIR regulators, the resonant part is used for the control of ac component with frequency ωowhile the integral part is used for the dc component. In our circuit, the dc and ac current component have the same state equation, so the coefficient of the resonant part is the same as the integral part with KR = KI. If there is no dc components in the phase current, the integral part can be removed and the regulator becomes a PR regulator with the transfer function GPR $i(s) = K$P + $2K$I$s/(s2 + \omega o2)$.The PWM of each cell is shifted to get better harmonic characters the same as the traditional cascaded H-bridge converters. So there is

$$S_{11} = S_{12} = \cdots = S_{1n} = S_1 \quad (10)$$

IV. SELF-BALANCING ABILITY OF THE CONVERTER

The control of the HF converters is the most important part of the control of the entire isolated dc/dc converter. In medium- or high-voltage applications, the switching frequency of the devices is limited while a high-frequency voltage is needed by the MWHF transformer. So square-wave modulation is usually used in this kind of converters [15], [29]–[34]. The square wave volt-age input to the windings can be shown in Fig. 4. A 50% duty symmetrical square wave is used to approach the fundamental sinusoidal wave and to reduce harmonics. If the switching frequency is much higher than the output voltage frequency, such as in using high speed MOSFET or SiC devices, the sinusoidal modulation can also be adopted.

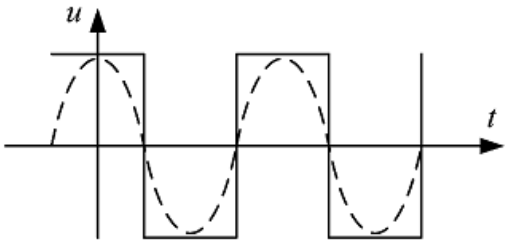


Fig. 4.Square wave voltage and its fundamental component on the transformer windings.

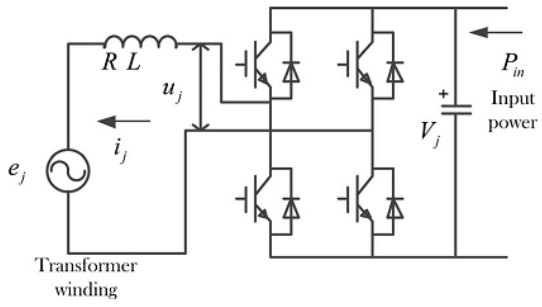


Fig. 5.Equivalent circuit of an HF converter and a transformer winding.

The stability and voltage self-balance ability of the circuit will be analyzed in this section. Suppose the switching states of the primary and secondary HF converters are all the same

$$S_{21} = S_{22} = \cdots = S_{2n} = S_{31} = S_{32} = \cdots = S_{3m} = S \quad (11)$$

Then the terminal voltages of *j*th HF converters can be written as

$$u_j = S.V_j \quad (12)$$

In the square-wave modulation mode, $S = \pm 1$. In sinusoidal modulation mode, $S = \sin \omega t$ with $-1 \leq S \leq 1$.

In previous introduction, the sum voltage of the dc buses of the CHBR is controlled by the strategy shown in Fig. 3. So each dc bus voltage can be controlled well if the voltage balance is realized.

To reduce the current ripples, filter inductors are used to link the HF converters and the transformer windings. The equivalent circuit of the *j*th winding and the HF converter can be expressed as in Fig. 5. Variable e_j is the back EMF in the *j*th transformer winding produced by the common flux. *R* and *L* are the equiv-alent values of the resistance and leakage inductance of the winding together with the filter inductance. All back EMFs can be considered as the same if neglecting the difference between windings of the transformer and the leak flux. Hence the voltage state equation in *j*th winding circuit is

$$u_j = Ri_j + L\frac{di_j}{dt} + e_j \quad (13)$$

Here $u_j = SV_j$.

Since the modulations of all HF converters are the same, the dc bus unbalance will cause the difference of the terminal voltages at the output port of the HF converter. Taking the *j*th and *k*th circuit as the example

$$\Delta u = u_j - u_k = S(V_j - V_k) \quad (14)$$

By (13), the voltage difference can also be written as

$$\Delta u = u_j - u_k = R(i_j - i_k) + L\frac{d(i_j - i_k)}{dt} \quad (15)$$

So we can get

$$S.\Delta V = R\Delta i + L\frac{d\Delta i}{dt} \quad (16)$$

with $V = V_j - V_k$ and $i = i_j - i_k$.

By the energy flow on the dc bus, the state equation of the *j*th dc bus voltage will be

$$\frac{1}{2}C\frac{dV_j^2}{dt} = P_{in} - P_{out} = P_{in} - S.V_j.i_j \quad (17)$$

where variable i_j is the output current of the HF inverters and P_{in} is the input power of the dc bus. P_{out} is the power flowing out of the dc bus through the HF converter. In the dc buses between the CHBR and the HF inverters, the direction of P_{in} is from the CHBR cells to HF inverters. On the load side, P_{in} is determined by the load power.

Equation (17) can be rewritten as

$$C\frac{dV_j}{dt} = \frac{P_{in}}{V_j} - S.i_j = P'_{in} - S.i_j \quad (18)$$

with $P_{in} = P_{in}/V_j$. By (18), the voltage difference between the *j*th and *k*th dc buses is

$$C\frac{d\Delta V}{dt} = \Delta P' - S.\Delta i \quad (19)$$

By (16) and (19) with $S = \pm 1$, the state equation of the dc voltages difference between the *j*th and *k*th dc bus is

$$\frac{d^2\Delta V}{dt} + \frac{R}{L}\frac{d\Delta V}{dt} + \frac{1}{LC}\Delta V = \frac{R\Delta P'}{L} \quad (20)$$

The characteristic equation of (20) is

$$S^2 + \frac{R}{L}s + \frac{1}{LC} = 0 \quad (21)$$

with the characteristic root

$$s = \left(-\left({}^{R}/_{L}\right) \pm \sqrt{\left(\frac{R}{L}\right)^2 - \left(\frac{4}{LC}\right)}\right)/2$$

which is also the decay time constant of the voltage difference ΔV.

When $(R/L)^2 > 4/LC$, the characteristic root is real and minus, the difference of the dc bus voltages will be reduced and finally converge to a constant value. That means the dc voltages have a natural balancing ability. To realize the natural balance and avoid oscillation, the dc bus capacitance, the inductance and resistance will satisfy

$$R > 2\sqrt{L/C} \qquad (22)$$

So the dc bus capacitance and resistance must be largee enough to produce the damp to make the dc bus voltagee difference converge to a constant value

The particular solution of the differential (20) is

$$\Delta V = RC\Delta P' \qquad (23)$$

which means when the load power is unbalanced, there will appear steady-state difference between the dc bus voltages as shown in (23). When the loads are balanced, all dc busvoltageswill be balanced naturally. In the CHBR, by (3), it is obvious that the power input to the dc bus is determined by the output voltage of each cell. Normally the input power of each cell is approximately balanced since a phase-shift PWM is adopted. So there is little dc voltage difference at the dc buses of the primary side. But in the secondary side, the load powers are different and normally are the output power of the dc bus, so there are voltage differences that are determined by the load power differences. Be that as it may, the load power difference may not lead to instability in the circuit. The voltage difference is determined by the resistance/dc bus capacitance and the load power unbalance. Specially, when the resistance is near zero, which means that the transformer can be regarded as an ideal voltage source, the voltage difference will be zero even there is some load imbalance. When the windings of the transformer are not exactly the same, there are differences between the back EMF and parameters such as inductance and resistance at different windings, the voltage difference of the dc buses will converge to a nonzero value, which is determined by the differences of back EMF and parameters of each winding.

V. ANALYSIS OF THE POWER EXCHANGE BETWEEN THETRANSFORMER WINDINGS

In the proposed converter, the unbalanced load may result voltage difference at the dc buses and will affect the stability of the converter. And the self-balancing speed is limited by the circuit parameters. So the voltage balance control method need to be studied to accelerate the voltage balancing and to eliminate the voltage difference caused by the power imbalance.Supposing that the number of cascaded modules of the CHBR is *n*, which is the same as the number of the primary winding of the transformer. The number of the secondary winding is *m*. The total number of the transformer windings is $N = n + m$.By energy balance principle, the state equation of one dc bus voltage is shown in (24)

$$\frac{d}{dt}\left(\frac{1}{2}CV^2\right) = P_i - P_0 \qquad (24)$$

Where$V$ is the dc bus voltage, C is the value of capacitance,$P_i$and $P_o$are the instantaneous input and output powers onthe dc bus. P_o also equals the power input into the transformer windings if ignoring the converter losses. The power flows are shown in Fig. 6. The filter inductance can be regarded as a part of the leak inductance of the transformer.The average value of the dc bus voltage is affected by the active power input to the dc capacitor. And the fluctuation of the dc bus voltage is affected by the reactive power. It means that the dc bus voltage can be realized by adjusting the active power injected into the dc capacitor.Since the carrier phase-shift PWM is used in CHBR, the active power input to each dc bus is fixed. The load power of the

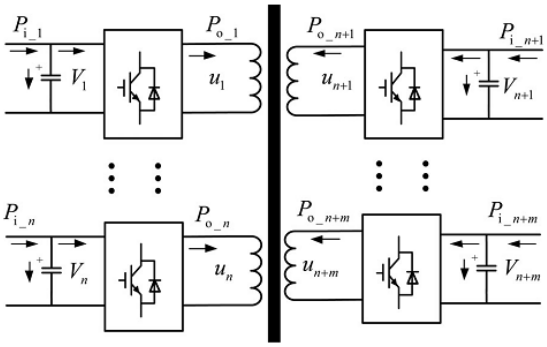


Fig 6 Power flow between all windings.

converter is determined by the loads. So the dc bus voltages can only be controlled by the active power flow from the dc buses to the transformer windings that can be controlled by the HF converters associated with the multiwindingtransformer.In the multiwinding transformer, all terminal voltages of the windings must have the same frequency to reduce the loss and harmonics. All windings are linked by the same flux if ignoring the leakage flux. The power can be transferred between the windings through the common flux, which can be used for the voltage balancing control. The energy exchange method will be studied in this section.The state equation in each winding of the transformer is

$$u - e = Ri + L\frac{di}{dt} \qquad (25)$$

Here u is the terminal voltage of the windings. Variable e is the back EMF produced by the flux. R and $L$are the resistance and inductance including the leak inductance of the winding and the filter inductance between the converter and the transformer. If ignoring the differences between the windings of the trans-former, the

back EMF and impedances are all the same. Then, the state equation of all windings can be shown as

$$u_1 - e = Ri_1 + L\frac{di_1}{dt}$$

$$u_2 - e = Ri_2 + L\frac{di_2}{dt}$$

$$u_{n+m} - e = Ri_{n+m} + L\frac{di_{n+m}}{dt} \quad (26)$$

By the Kirchhoff law, the sum of the currents input the trans-former is zero

$$\sum i_i = 0 \quad (27)$$

Adding all equations in (26)

$$\frac{1}{N}\sum_{i=1}^{N} u_i - e = 0 \quad (28)$$

That means the back EMF in the transformer winding is determined by the sum of the terminal voltages.Taking the *j*th windings as an example, its state equation is

$$u_j - e = R.i_j + L\frac{di_j}{dt} \quad (29)$$

Supposing the back EMF in the winding is

$$e = \frac{1}{N}\sum u_i = ucos(\omega t + \theta_e) \quad (30)$$

And the terminal voltage in the *j*th winding is

$$u_j = (u + \Delta u)cos(\omega t + \theta_j) \quad (31)$$

Here $\omega = 2\pi f$ is the frequency of the terminal voltages. $\theta$and$\theta j$are the phases of the back EMF and the terminal voltage. The terminal voltage is determined by the HF converters. Ignoring the resistance of the windings, the current in the *j*th winding can be obtained by (29)–(31)

$$i_j = \frac{2u}{\omega L} sin\frac{\theta_j - \theta_e}{2}\cos\left(\omega t + \frac{\theta_j - \theta_e}{2}\right) + \frac{\Delta u}{\omega L}\sin(\omega t + \theta_j) \quad (32)$$

In the proposed circuit, the transformer has functions of isolation and energy balancing ability between each cell.

Also in the proposed converter, the unbalanced load may result voltage difference at the dc buses and will affect the stability of the converter. And the self-balancing speed is limited by the circuit parameters.

Then the instantaneous power output of the*j*th dc bus is

$$P_{o-j} = u_j i_j = \frac{u^2 + u\Delta u}{2\omega L}\sin(\theta_j - \theta_e) + \frac{u^2 + u\Delta u}{\omega L} \times sin\frac{\theta_j - \theta_e}{2}\cos\left(2\omega t + \frac{3\theta_j - \theta_e}{2}\right) + \frac{u.\Delta u + \Delta u^2}{2\omega L}\sin(2\omega t + 2\theta_j) \quad (33)$$

The active power output of the *j*th dc bus is

$$P_{oa-j} = \frac{u^2 + u\Delta u}{2\omega L}\sin(\theta_j - \theta_e) \quad (34)$$

The active power will affect the average value of the dc bus voltage. The other parts in (33) are the reactive power that will only produce fluctuations on the dc voltage. By (33), the input active power to the transformer windings is determined by the phase difference between the terminal voltage and the back EMF. In the medium- or high-voltage applications, square-wave modulation is usually adopted because of the limitation of the switching frequency. The square wave voltage input to the windings is shown in Fig. 4. By Fourier analysis, the square wave voltage is composed by a group of sinusoidal components with different frequencies. So the voltage and current in the windings can also be expressed as

$$u = \sum u_k \cos(k\omega t + \theta_k)$$

$$i = \sum i_k \cos(k\omega t + \phi_k) \quad (35)$$

Here k is an integer number that stands for the harmonic number. The active power produced by different frequency voltage and current is

$$P_a = \int_o^T u_k \cos(k\omega t + \theta_k) \cdot i_l \cos(l\omega t + \phi_l) dt \qquad (36)$$

If $k = l$, there is $P_a = 0$

We know that only the voltage and current with the same frequency can produce active power. The active power input can be controlled by adjusting the phase angle of the voltage at each harmonic angular frequency $k\omega$. When the square wave voltage is symmetrical, the fundamental component is obviously the largest. On the other hands, from

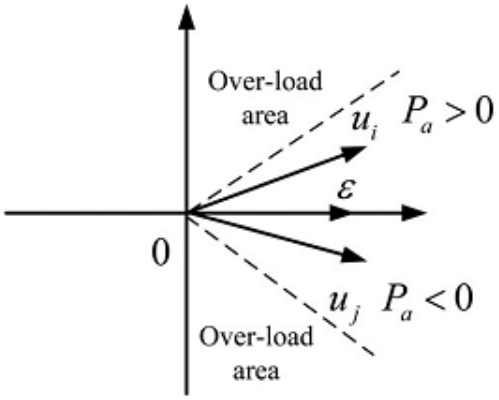


Fig. 7.Output power control by phase adjustment.

(34), it is obvious that the active power is decreasing with the increase of the frequency. So the power flow between the windings is determined by the fundamental component whose phase is also the same with the symmetrical square wave. That means the active powers are also determined by the phase of the square wave voltage.

VI. VOLTAGE BALANCE CONTROL

From (33) we can see that if there is no phase difference between the terminal voltage and back EMF, the output active power of this winding will be zero even if there is an amplitude difference. It means that only phase of the terminal voltage can be used for active power control. To be simple, the same modulation method is used for all HF inverters and HF rectifiers in the isolated dc–dc converter, except the difference of phase. So all the terminal voltages of the transformer windings have same amplitudes when the dc buses are balanced. As in the former analysis, the dc bus voltage can be adjusted by the re-distribution of the input and output power between the transformer windings, which can be realized by the adjustment of the phase angles of the terminal voltages. By (33), if voltage *uj*is phase-lead of the back EMF with $\theta j > \theta e$, the active power is flowed from the dc bus to the transformer. If voltage *uj*is phase-lag with $\theta j < \theta e$, the active power is flowed from the transformer winding to the dc bus. The active power reaches the peak value when phase difference is $\pm\pi/2$. By (32) and (33), the current and reactive power of the windings are also affected by $\theta j - \theta e$. Also the reactive power will reach its peak value with the phase difference of $\pm\pi$ while the input current will also reach its peak value. In the transformer, normally there is $E \ \omega L \cdot I$ to reduce the loss and to make full use of the magnet where E is the rated value of the back EMF. Then, there is

$$\frac{U}{\omega L} \gg 1 \qquad (37)$$

Here *U*and*I*are the rated voltage and current of the windings. According to (32), if the phase difference increases, the current and power passing the winding will increase quickly and overload will occur that will damage the transformer and converters. As the increase of the reactive power, the fluctuations of the dc bus voltages will increase, which will reduce the performance of the converter. So the phase difference is normally controlled to be little difference to avoid over-current and over-load, as shown in Fig. 7.

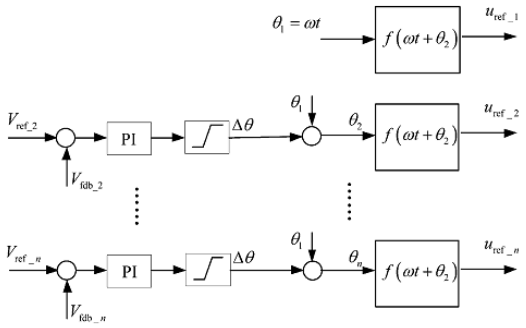


Fig. 8. PI regulators to get the control phase angles.

Because the summarized dc bus voltage connected with the CHBR is already controlled by the control scheme shown in Fig. 3, only $n + m - 1$ dc buses are needed to be controlled directly by separate voltage balance controllers. These $n + m - 1$ dc buses are

named directly-controlled dc buses. The last one can be balanced naturally if the summarized dc buses voltage and the $n + m - 1$ buses are all controlled well. So it can be named as indirectly-controlled dc bus. The voltage difference is nonlinear with the phase difference angle, also the angle of the back EMF is difficult to be got directly, so a PI regulator for the dc voltage feedback is used where the phase difference with the back EMF is adaptively obtained. In practice, the output voltage phase on the first dc bus $\theta 1$ is used as a reference. Then, a group of PI regulators are used to get the phase angle of the terminal voltages on the other windings. The difference of the dc bus voltages and their reference values are used as the input of the PI regulators, as shown in Fig. 8. The output is the phase difference to the first cell. By the adaptability of the PI regulator, the difference between the windings, such as the back EMF and impedance difference, can be compensated by the close-loop control. Since the input active powers from the CHBR are almost the same because of the carrier phase-shift PWM, the required phase difference of the terminal voltages on the primary windings is little. But the voltage phases on the secondary windings may be quite different depends on the loads imbalance.

VII. EXPERIMENTAL RESULTS

To verify the performance of the proposed converter topologyand the voltage balancing method, an experimental platform is set up in the lab as shown in Fig. 9. The transformer has two primary windings and two secondary windings, whose rated power is 4 kVA. The MOSFET IRF640 of 200 V and 18 A are used as the switching devices. The reference voltage of each dc bus is set to be 40 V, which is enough to test the effects of the control algorithm. TI DSP of TMS320F28335 is used as the core controller and a number of CPLDs are used as the PWM expansion for all converters. Symmetric square-wave

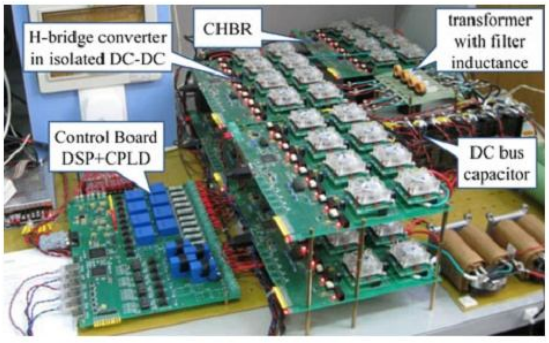


Fig. 9.Experimental platform.

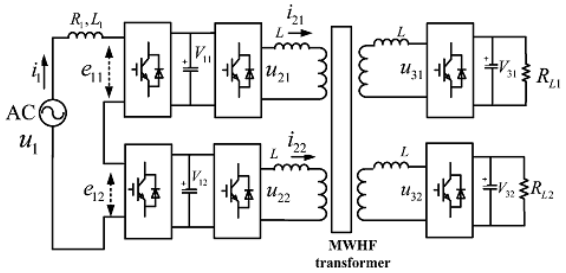


Fig. 10.Circuit of the experimental platform.

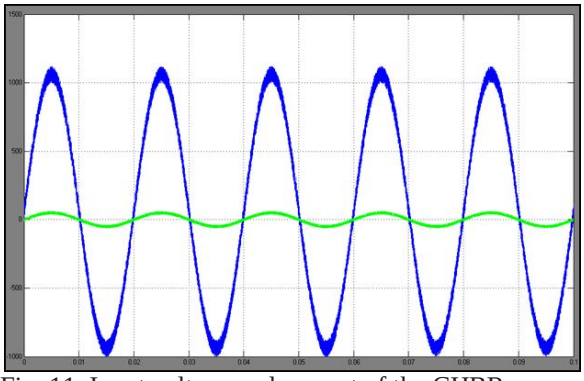


Fig. 11. Input voltage and current of the CHBR.

modulation is used with the frequency of 20 kHz, which is also the HF converter switching frequency. The electrical circuit of the platform is shown in Fig. 10. Some resistors are connected on the dc buses output by the HF rectifiers to simulate the loads. The input voltage and current of the *H*-bridge rectifier are shown in Fig. 11. It shows that the input current is almost the same phase with input voltage and the power factor can be controlled well. Without the voltage balancing control, all output voltages of the four HF converters are controlled by the same PWM modulation without phase difference, the output voltages and

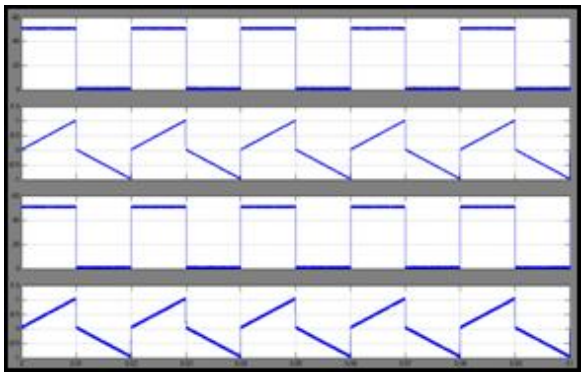
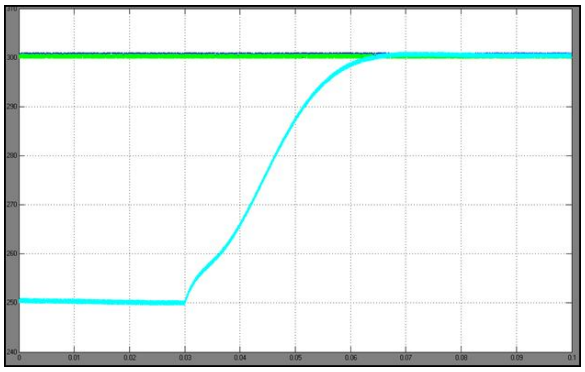


Fig. 12.Output voltage and current of the HF converter.

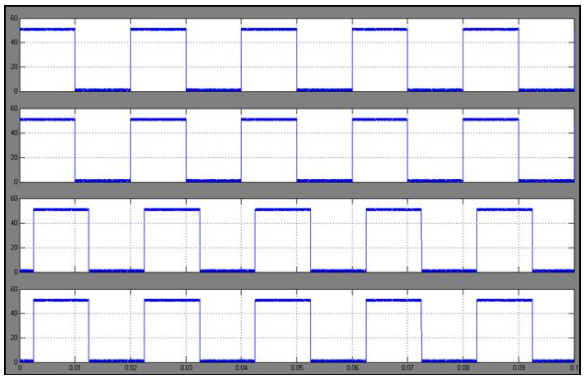
currents of the HF inverters are shown in Fig. 12. Since

the square modulation is adopted and the circuit resistance is little, the current is almost linearly increase or decrease affected by the terminal voltages. When the same loads are driven on the secondary side, the four dc bus voltages are shown in Fig. 16. Since the input powers at the primary side are controlled the same and positive by the CHBR, the dc bus voltages $V11$ and $V12$ are almost the same. The powers on the secondary sides are negative and also balanced, so the two dc buses

$V31$ and $V32$ are also balanced. Since the input power on the primary side is positive and the input power on the secondary side is negative, the dc bus voltages $V11V12$ are larger than $V31V32$. It has verified that the voltage difference is determined by the power difference input into the dc buses as shown in (23). The experimental results are also similar to the simulation results.
When the loads are unbalanced at secondary side, the dc voltages on secondary side will become different. The voltage difference is determined by the power difference in (23), but the circuit is still stable and can continue to work. The stability of the circuit is verified.



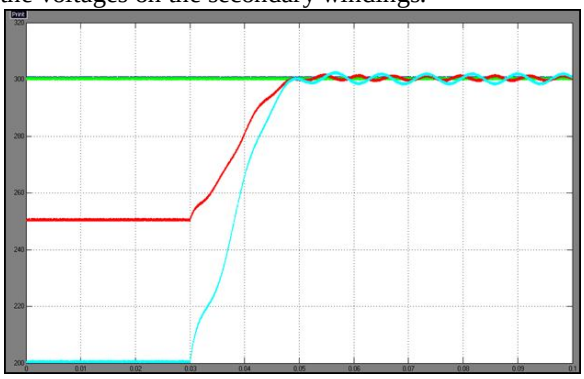
(a)



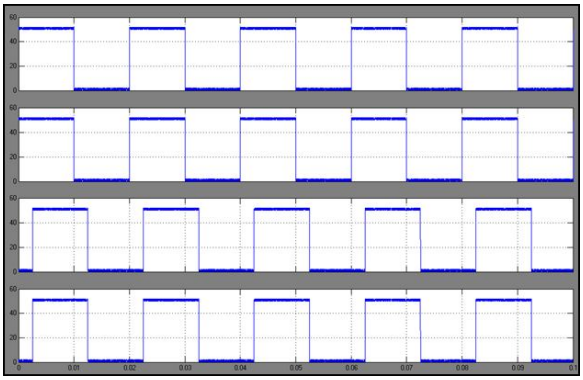
(b)

Fig. 13. Voltage control results with balance load. (a) DC bus voltage balancecourse with balanced load. (b) Terminal voltages in steady state with balanced loads.

Using the voltage balancing control proposed in this paper,the voltage balance control results are shown in Fig. 13(a).Fig. 13(b) is the terminal voltages of the HF converters. The first and second waveforms are the voltage on the primary windings.The third and fourth are the voltages on the secondary windings.



(a)



(b)

Fig. 14. Voltage balance control results with unbalance load. (a) Balance course with unbalanced load. (b) Terminal voltages in steady state with unbalanced load

Because the power flows in the cells of the CHBR are almost the same, u_{21} and u_{22} are almost with the same phase. The loads on the secondary windings are also balanced, so u_{31} and u_{32} are also with the same phases. The phase of voltages u_{21} and u_{22} are leading the others, which means the power is flowing from the primary side to the secondary side.
When unbalanced loads are driven on the dc buses of the secondary side, the dc buses voltages will be different because of the power unbalance. The load on V_{31} is

larger than V_{32}, so the dc voltage of V_{31} is smaller than V_{32} if the voltage balance control algorithm is not used. When the proposed voltage balance control methods are used, the bus voltages will be balanced quickly as shown in Fig. 14(a). The steady-state terminal voltages of the HF converters with unbalanced loads are shown in Fig. 14(b). The phase of u_{31} has more phase lag than u_{32} to fit the larger loads.

VIII. CONCLUSION

The proposed multilevel converter can be applied in mediumor high-voltage applications. It is modular and is of the characteristics of high reliability. The HF transformer significantly reduces the system weight and volume compared with the industry-frequency transformer. The HF multi winding transformer can also realize the power redistribution and voltage balancing control. A voltage balancing control method based on terminal voltage phase adjustment is studied in this paper. Simulations and experimental have been implemented to verify the stability without control. It shows that the proposed circuit can be controlled stable and reliable under unbalanced loads.

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