

LOW POWER DOUBLE-TAIL COMPARATOR USING SWITCHING TRANSISTORS

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Abstract: Comparator is one of the fundamental building blocks in most analog to digital converters. Many high speed analog to digital converters such as flash analog to digital converter require high speed and low power comparators. A new double tail comparator is designed, where the circuit of a conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors the positive feedback during the regeneration is strengthened which results in remarkably reduced delay time. Post layout simulation results in a 0.18 μ m technology confirm the analysis results. It is shown that in the switching transistors using dynamic comparator, both the power consumption and delay time are significantly reduced. Power consumption of conventional double tail comparator is 12 μ W in 0.8v and power is reduced to 9.5 μ W in double tail comparator using switching transistors with the same supply voltage.

Keywords—Double tail comparator, dynamic clocked comparator, high speed analog to digital converters, low power analog design, switching transistor.

I. Introduction

The Comparators are used in analog-to-digital converters (ADCs), data transmission applications, switching power regulators and many other applications. The voltages that appear at the inputs are compared by the comparator that produces a binary output which represents a difference between them. They are critical components in analog-to-digital converters. Designing high-speed comparators becomes more challenging when working with smaller supply voltages. In other words, for a

given technology, to attain high speed, transistors with increased width and length values are required to compensate for the reduction of supply voltage, which also means increased chip area and power [1]. So, Transistor width and length are adjusted accordingly for minimum power consumption and maximum operating speed. Hysteresis in the comparator circuit is applied by feeding back a small portion of the output voltage to the positive input [2].

This feedback voltage adds a polarity-sensitive offset to the input, which results in increased threshold range. A small amount of hysteresis applied to the comparator circuit can prove to be very useful as it reduces the circuit's sensitivity to noise, and also helps reduce multiple transitions occurring at the output if the input is slowly changing its state.

A model for the comparator is developed and discussed, and its functionality is verified by showing a comparison of result obtained for the proposed model and the existing model. The platform used to develop and analyze the existing model is tanner eda tool.

The research paper is organized as follows: an introduction to CMOS comparator is given, followed by detailed analysis of high speed comparator architecture with properties for each structure will be discussed. Finally, simulation result for all the architecture will be shown and discussed.

II. Material and Methodology

A clocked comparator is a circuit element that makes decision as to whether the input signal is high or low at every clock cycle. Clocked regenerative comparators make fast decision due to strong positive feedback in the regenerative latch. Here analyse the delay of single tail comparator, double tail comparator and proposed comparator.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK=0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK=VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD – |Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuit works vice versa. As shown in Fig. 2, the delay of this comparator is comprised of two time delays, t0 and tlatch. The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e., VINP > VINN), the drain current of transistor M2 (I2) causes faster discharge of Outp node compared to the Outn node, which is driven by M1 with smaller current. Consequently, the discharge delay (t0) is given by

$$t_0 = \frac{C_L |V_{thp}|}{I_2} \cong 2 \frac{C_L |V_{thp}|}{I_{tail}}$$

In (1), since $I_2 = I_{tail} \frac{\beta_1}{\beta_1 + \beta_2} + I_{in}$ and $I_{in} = I_{tail} \frac{\beta_2}{\beta_1 + \beta_2} - g_{m1,2} V_{in}$, for small differential input

(V_{in}), I_2 can be approximated to be constant and equal to the half of the tail current. The second term, t_{latch} , is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of $V_{out} = V_{DD}/2$ has to be obtained from an initial output voltage difference V_0 at the falling output (e.g., Outp). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch. Hence, the latch delay time is given by,

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln \left(\frac{\Delta V_{out}}{\Delta V_0} \right) = \frac{C_L}{g_{m,eff}} \cdot \ln \left(\frac{V_{DD}/2}{\Delta V_0} \right)$$

Where $g_{m,eff}$ is the effective transconductance of the back-to back inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at $t = t_0$). Based on (1), V_0 can be calculated from (3)

$$\begin{aligned} \Delta V_0 &= |V_{outp}(t = t_0) - V_{outn}(t = t_0)| \\ &= |V_{thp}| - \frac{I_2 t_0}{C_L} = |V_{thp}| \left(1 - \frac{I_2}{I_1} \right). \end{aligned}$$

The current difference, $\Delta I_{in} = |I_1 - I_2|$, between the branches is much smaller than I_1 and I_2 . Thus, I_1 can be approximated by $I_{tail}/2$ and (3) can be rewritten as

$$\begin{aligned} \Delta V_0 &= |V_{thp}| \frac{\Delta I_{in}}{I_1} \\ &\approx 2 |V_{thp}| \frac{\Delta I_{in}}{I_{tail}} \\ &= 2 |V_{thp}| \frac{\sqrt{\beta_{1,2}} I_{tail}}{I_{tail}} \Delta V_{in} \\ &= 2 |V_{thp}| \sqrt{\frac{\beta_{1,2}}{I_{tail}}} \Delta V_{in}. \end{aligned}$$

In this equation, $\beta_{1,2}$ is the input transistors' current factor and I_{tail} is a function

of input common-mode voltage (V_{cm}) and V_{DD} . Now, substituting t_0 in latch delay expression and considering t_0 , the expression for the delay of the conventional dynamic comparator is obtained as

$$t_{delay} = t_0 + t_{latch}$$

$$= 2 \frac{C_L |V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln \left(\frac{V_{DD}}{4 |V_{thp}| \Delta V_{in} \sqrt{\beta_{1,2}}} \sqrt{\frac{I_{tail}}{\beta_{1,2}}} \right)$$

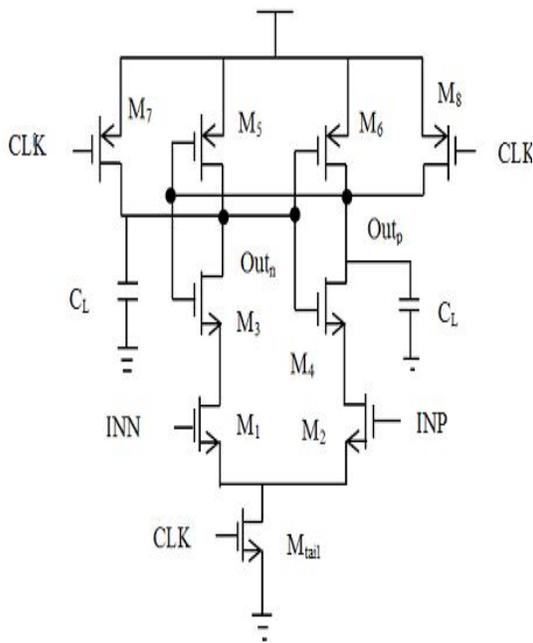
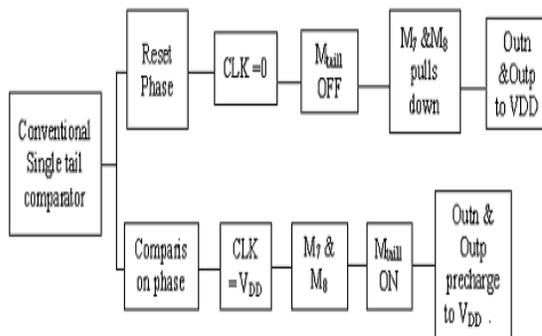


Fig :1.1 Schematic diagram of conventional single tail comparator



Equation (5) explains the impact of various parameters. The total delay is directly proportional to the comparator load capacitance C_L and inversely proportional to the input difference voltage (V_{in}). Besides, the delay depends indirectly to the input common-mode voltage (V_{cm}). By reducing V_{cm} , the delay t_0 of the first sensing phase increases because lower V_{cm} causes smaller bias current (I_{tail}). On the other hand, (4) shows that a delayed discharge with smaller I_{tail} results in an increased initial voltage difference (V_0), reducing t_{latch} . Simulation results show that the effect of reducing the V_{cm} on increasing of t_0 and reducing of t_{latch} will finally lead to an increase in the total delay. In [17], it has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M_3 and M_4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M_5 or M_6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M_3 and M_4 , where the gate-source voltage of M_5 and M_6 is also small; thus, the delay time of the latch becomes large due to lower transconductances

Another important drawback of this structure is that there is only one current path,

via tail transistor M_{tail} , which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better G_m/I ratio, a large tail current would be desirable to enable fast regeneration in the latch. Besides, as far as M_{tail} operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

B. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 3. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider M_{tail2} , for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}), for low offset.

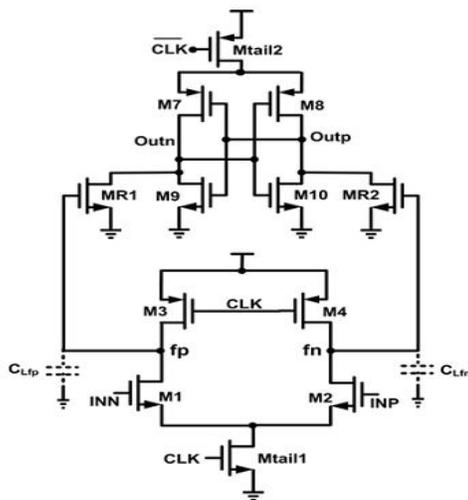
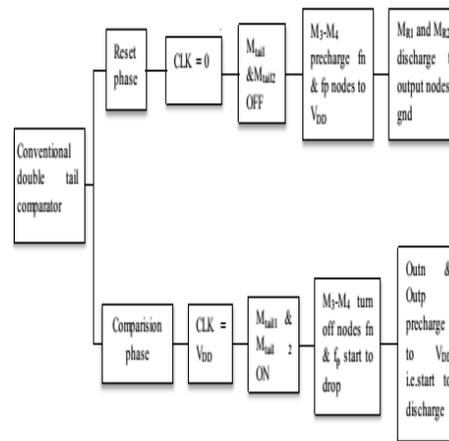


Fig. 3. Schematic diagram of the conventional double-tail dynamic comparator



The operation of this comparator is as follows (see Fig. 4). During reset phase ($CLK=0$, M_{tail1} , and M_{tail2} are off), transistors M_3 - M_4 pre-charge fn and fp nodes to V_{DD} , which in turn causes transistors MR_1 and MR_2 to discharge the output nodes to ground. During decision-making phase ($CLK = V_{DD}$, M_{tail1} and M_{tail2} turn on), M_3 - M_4 turn off and voltages at nodes fn and fp start to drop with the rate defined by $I_{M_{tail1}}/C_{fn}(p)$ and on top of this, an input-dependent differential voltage $V_{fn}(p)$ will build up. The intermediate stage formed by MR_1 and MR_2 passes $V_{fn}(p)$ to the cross-coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t_0 and t_{latch} . The delay t_0 represents the capacitive charging of the load capacitance C_{Lout} (at the latch stage output nodes, $Outn$ and $Outp$) until the first n-channel transistor (M_9/M_{10}) turns on, after which the latch regeneration starts; thus t_0 is obtained from

$$t_0 = \frac{V_{Thn} C_{Lout}}{I_{B1}} \approx 2 \frac{V_{Thn} C_{Lout}}{I_{tail2}}$$

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.

1) The voltage difference at the first stage outputs ($V_{fn/fp}$) at t_{met0} has a profound effect on latch initial differential output voltage (V_0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.

2) In this comparator, both intermediate stage transistors will be finally cut-off, (since f_n and f_p nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to V_{DD} , which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III. Proposed Double-Tail Dynamic Comparator

Fig. 5 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase $V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, two control transistors (M_{c1} and M_{c2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner [see Fig. 5(a)].

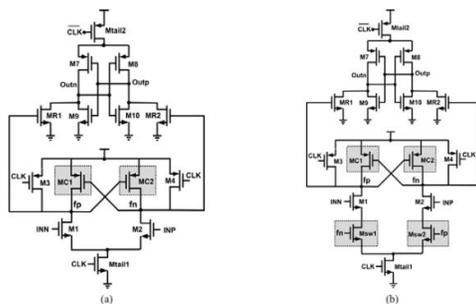


Fig. 5. Schematic diagram of the proposed dynamic comparator. (a) Main idea. (b) Final structure

A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows (see Fig. 6). During reset phase ($CLK=0$, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pull both f_n and f_p nodes to V_{DD} , hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2} , reset both latch outputs to ground. During decision-making phase ($CLK=V_{DD}$, M_{tail1} , and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since f_n and f_p are about V_{DD}). Thus, f_n and f_p start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus f_n drops faster than f_p , (since M_2 provides more current than M_1). As long as f_n continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling f_p node back to the V_{DD} ; so another control transistor (M_{c2}) remains off, allowing f_n to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $V_{fn/fp}$ is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node f_n discharges faster, a pMOS transistor (M_{c1}) turns on, pulling the other node f_p back to the V_{DD} . Therefore by the time passing, the difference between f_n and f_p ($V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from V_{DD} is drawn to the ground via input and tail transistor (e.g., M_{c1} , M_1 , and M_{tail1}), resulting in static power consumption. To overcome this issue, two nMOS switches are

used below the input transistors [Msw1 and Msw2, as shown in Fig. 5(b)].

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch. This will be more discussed in the following section.

B. Delay Analysis

In order to theoretically demonstrate how the delay is reduced, delay equations are derived for this structure as previously done for the conventional dynamic comparator and the conventional double-tail dynamic comparator. The analysis is similar to the conventional double-tail dynamic comparator, however; the proposed dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (V_0) at the beginning of the regeneration ($t = t_0$); and second, it enhances the effective transconductance (g_{meff}) of the latch. Each of these factors will be discussed in detail.

1) Effect of Enhancing V_0 :

As discussed before, we define t_0 , as a time after which latch regeneration starts. In other words, t_0 is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it

will pull down one of the outputs and regeneration will commence. According to (2), the latch output voltage difference at time t_0 , (V_0) has a considerable impact on the latch regeneration time, such that bigger V_0 results in less regeneration time. Similar to the equation derived for the V_0 of the double-tail structure, in this comparator we have

$$\begin{aligned} \Delta V_0 &= V_{Thn} \frac{\Delta I_{latch}}{I_{B1}} \\ &\approx 2V_{Thn} \frac{\Delta I_{latch}}{I_{tail2}} \\ &= 2V_{Thn} \frac{g_{mR1,2}}{I_{tail2}} \Delta V_{fn/fp}. \end{aligned}$$

In order to find $V_{fn/fp}$ at $t = t_0$, we shall notice that the combination of the control transistors (Mc1 and Mc2) with two serial switches (Msw1, Msw2) emulates the operation of a back-to-back inverter pair; thus using small-signal model presented, $V_{fn/fp}$ is calculated by

$$\Delta V_{fn/fp} = \Delta V_{fn(p)0} \exp((A_v - 1)t/\tau).$$

2) Effect of Enhancing Latch Effective Transconductance:

As mentioned before, in conventional double-tail comparator, both fn and fp nodes will be finally discharged completely. In our proposed comparator, however, the fact that one of the first stage output nodes (fn/fp) will charge up back to the VDD at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words, positive feedback is strengthened.

By comparing the expressions derived for the delay of the three mentioned structures, it can be seen that the proposed comparator takes advantage of an inner positive feedback in double-tail operation, which strengthens the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of V_{Th}/VDD , the

transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator. Simulation results confirm this matter.

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \cdot \ln \left(\frac{\Delta V_{out}}{\Delta V_0} \right) = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \cdot \ln \left(\frac{V_{DD}/2}{\Delta V_0} \right). \quad (16)$$

Finally, by including both effects, the total delay of the proposed comparator is achieved from

$$t_{delay} = t_0 + t_{latch} = 2 \frac{V_{Thn} C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \cdot \ln \left(\frac{V_{DD}/2}{\Delta V_0} \right) = 2 \frac{V_{Thn} C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \times \ln \left(\frac{V_{DD}/2}{4V_{Thn} |V_{Thp}| \frac{g_{mR1,2}}{I_{tail2}} \frac{g_{m1,2} \Delta V_{in}}{I_{tail1}} \exp \left(\frac{G_{m,eff1} \cdot t_0}{C_{L,fn(p)}} \right)} \right). \quad (17)$$

3) Reducing the Energy per Comparison:

It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. As discussed earlier, in conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the VDD. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required. This can be seen when being compared with conventional topologies.

IV. Simulation Results And Comparison

The proposed circuit was simulated using Tanner EDA tool with 180nm

technology. The supply voltage used in simulation is 1.8 volt. From table 1 it is visible that average power consumption, EDP and PDP of proposed comparator reduced.

Fig. 6 shows the simulation result of the proposed comparator and the power result of the proposed comparator is shown in Fig. 7

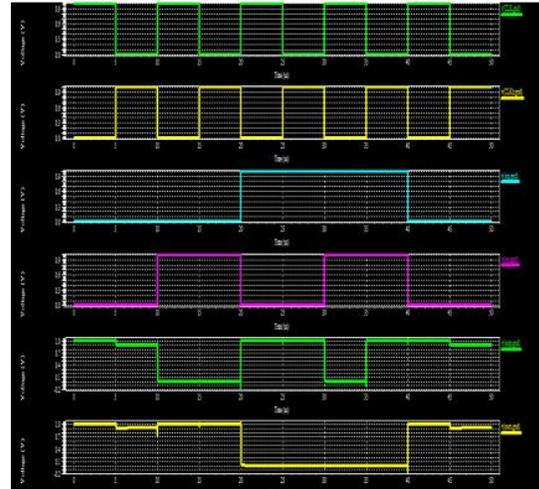


Fig.6 Simulation Result of Proposed Comparator

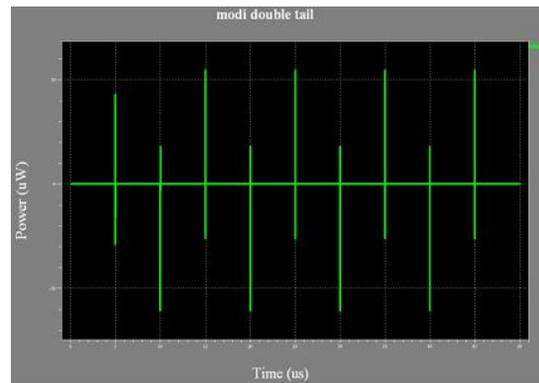


Fig.7 Power Result of Proposed Comparator.

V. Conclusion:

In this paper, an analysis for clocked dynamic comparators is presented. One structure of double-tail dynamic comparators was analysed. Also, based on analyses, a new dynamic comparator with low-voltage lowpower capability was proposed in order



to improve the performance of the comparator. Simulation results in 0.18- μm CMOS technology confirmed that the delay and power consumption of the proposed comparator is reduced to a great extent in comparison with the existing double-tail comparator.

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