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DESIGN AND SIMULATION OF A NOVEL DSTATCOM TOPOLOGY FOR LOAD COMPENSATION WITH WEAK SOURCE

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ABSTRACT- In this paper, a new topology for DSTATCOM applications with non stiff source is proposed. The proposed topology enables DSTATCOM to have a reduced dc-link voltage without compromising the compensation capability. It uses a series capacitor along with the interfacing inductor and a shunt filter capacitor. With the reduction in dc-link voltage, the average switching frequency of the insulated gate bipolar transistor switches of the DSTATCOM is also reduced. Consequently, the switching losses in the inverter are reduced. Detailed design aspects of the series and shunt capacitors are discussed in this paper. A simulation study of the proposed topology has been carried out using MATLAB/SIMULINK and the results are presented.

Index Terms— DC-link voltage, distribution static compensator (DSTATCOM), hybrid topology.

I. INTRODUCTION

THE proliferation of power electronics devices, nonlinear loads, and unbalanced loads has degraded the power quality in the power distribution network [1]. To improve the quality of power, active power filters have been proposed [2]–[4]. The distribution static compensator (DSTATCOM) is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. In practice, the load is remote from the distribution substation and is associated with feeder impedance. In the presence of feeder impedance, the inverter switching's distort both the PCC voltage and the source currents. In this situation, the source is termed as non stiff. If the same control algorithm for the stiff sources is used for the non stiff sources, the reference currents generated will be erroneous; the load compensation using state feedback control of DSTATCOM with shunt filter capacitor gives, however, better results [5], [6]. The state feedback control of the shunt filter capacitor eliminates the switching frequency components in the terminal voltages and source currents.

The compensation performance of any active filter depends on the voltage rating of dc-link capacitor [7]. In general, the dc-link voltage has much higher value than the peak value of the line-to-neutral voltages. This is done in order to ensure a proper compensation at the peak of the source voltage. In [8], the authors discuss the current distortion limit and loss of control limit, which states that the dc-link voltage should be greater than or equal to $\sqrt{6}$ times the phase voltage of the system for distortion-free compensation. When the dc-link voltage is less than this limit, there is insufficient resultant voltage to drive the currents through the inductances so as to track the reference currents. Reference value of the dc-bus capacitor voltage mainly depends upon the requirement of reactive power compensation of the active power filter. The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak of source voltage at the PCC. Due to these criteria, many researchers have used a higher value of dc capacitor voltage based on their applications.

With the high value of dc-link capacitor, the voltage source inverter (VSI) becomes bulky and the switches used in the VSI also need to be rated for higher value of voltage and current. This, in turn, increases the entire cost and size of the VSI. A few attempts have been made in the literature to reduce the dc link\ voltage storage capacity. In [18] and, a hybrid filter has been discussed for motor drive applications. The filter is connected in parallel with diode rectifier and tuned at seventh harmonic frequency. Although an elegant work, the design is specific to the motor drive application and the reactive power Compensation is not considered, which an important aspect

Fig. 2 shows the equivalent circuit of the proposed

in DSTATCOM applications is.

In this paper, a new DSTATCOM topology with reduced dc link voltage is proposed. The topology consists of two capacitors: one is in series with the interfacing inductor of the active filter and the other is in shunt with the active filter. The series capacitor enables reduction in dc-link voltage while simultaneously compensating the reactive power required by the load, so as to maintain unity power factor without compromising DSTATCOM performance. The shunt capacitor, along with the state feedback control algorithm, maintains the terminal voltage to the desired value in the presence of feeder impedance.

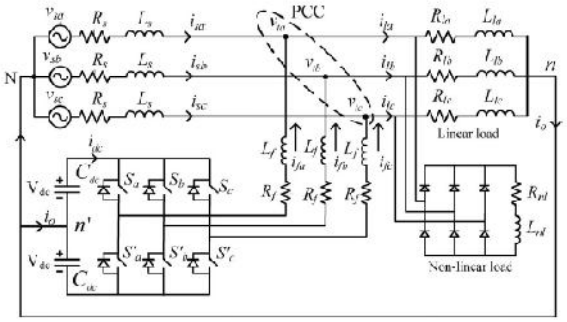


Fig.1. Equivalent circuit of the neutral clamped VSI topology-based DSTATCOM.

II. OLD AND NEW TOPOLOGIES OF DSTATCOM

In this section, the conventional and proposed topologies of the DSTATCOM are discussed in detail. Fig. 1 shows the power circuit of the neutral clamped VSI topology-based DSTATCOM which is considered the conventional topology in this study. Even though this topology requires two dc storage devices, each leg of the VSI can be controlled independently and tracking is smooth with less number of switches when compared to other VSI topologies. In this figure, v_{sa}, v_{sb} , and v_{sc} are source voltages of phases *a*, *b*, and *c*, respectively. Similarly, v_{ta} , v_{tb} , and v_{tc} are the terminal voltages at the PCC. The source currents in three phases are represented by i_{sa} , i_{sb} , and i_{sc} and load currents are represented by i_{la} , i_{lb} , and i_{lc} .

The shunt active filter currents are denoted by i_{fa}, i_{fb}, i_{fc}, and i_o represents the current in the neutral leg. *Ls* and *Rs* represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance are represented by L_f and R_f , respectively. The load constituted of both linear and nonlinear loads are as shown in this figure. The dc-link capacitors and voltages across them are represented by $C_{dc1} = C_{dc2} = C_{dc}$ and $V_{dc1} = V_{dc2} = V_{dc}$, respectively. The current through the dc link is represented by the i_{dc}. In this topology, the voltage across each dc-link capacitance is chosen as 1.6 times the peak value of the source voltages.

neutral clamped VSI topology-based DSTATCOM. It is a combination of the conventional DSTATCOM topology with a capacitor C_f in series with the interfacing shunt branch of the active filter and a capacitor C_{sh} in shunt with the active filter. This topology is referred to as hybrid topology. The passive capacitor C_f has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load.

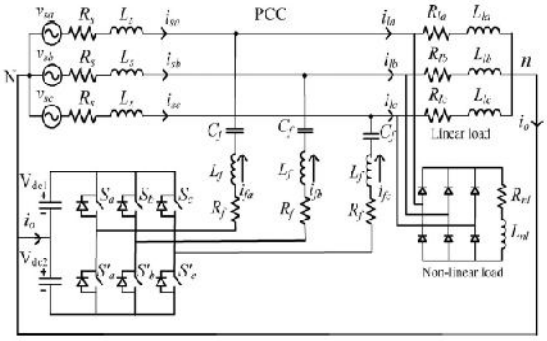


Fig. 2. Equivalent circuit of the proposed neutral clamped VSI topology-based DSTATCOM (hybrid filter).

The addition of capacitor in series with the interfacing inductor of the conventional topology will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section. The shunt capacitor C_{sh} largely eliminates the switching frequency components of the VSI in the terminal voltages and source currents using state feedback control. The design of the series capacitor C_f and the shunt capacitor C_{sh} have significant effect on the performance of the compensator.

III. STATE FEEDBACK CONTROL METHOD

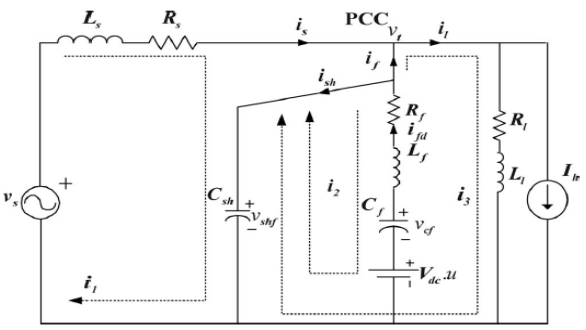


Fig. 3. Single-line diagram of the proposed DSTATCOM.

The single-line diagram of the proposed DSTATCOM is shown in Fig. 3. To derive the state-space model of the system in Fig. 3, we choose five local variables (i.e., three loop currents and two capacitor voltages). Now, the state vector is defined as follows:

$$x = [i_1\ i_2\ i_3\ v_t\ v_{cf}]^t \quad (1)$$

The circuit shown in Fig. 3 contains three forcing functions: the source voltage v_s, the nonlinear load current I_h, and switching variable u. The u is replaced by the continuous time variables u_c and the control vector is defined as

$$u = [u_c] \quad (2)$$

The state-space equation of the circuit can be written as

$$\dot{x} = Ax + B_1 v_s + B_2 u + B_3 I_h \quad (3)$$

Where

$$A = \begin{bmatrix} -R_s/L_s & 0 & 0 & -1/L_s & 0 \\ 0 & -R_f/L_f & 0 & 1/L_f & -1/L_f \\ 0 & 0 & -R_l/L_l & 1/L_f & 0 \\ 1/C_{sh} & -1/C_{sh} & -1/C_{sh} & 0 & 0 \\ 0 & 1/C_f & 0 & 0 & 0 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1/L_s \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, B_2 = \begin{bmatrix} 0 \\ -V_{dc}/L_f \\ 0 \\ 0 \\ 0 \end{bmatrix}, B_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ -1/C_f \\ 0 \end{bmatrix}$$

The state variables can be written as network parameters as follows:

$$i_{s=i_1};\ i_{sh} = i_1 - i_2 - i_3;$$

$$i_f = i_3 - i_1;\ v_{cf} = v_{cf};\ v_{shf} = v_t. \quad (4)$$

A transformed state vector z, which relates the state vector x with the network parameters using (8), can be written as

$$z = \begin{bmatrix} i_f \\ i_{sh} \\ i_l \\ v_l \\ v_{cf} \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 & 0 & 0 \\ 1 & -1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} x = Px. \quad (5)$$

The state-space representation of the system given in (7) is transformed by using (9) as

$$\dot{z} = PAP^{-1}z + PB_1 v_s + PB_2 v_s + PB_3 I_h$$
$$= \Lambda z + \Gamma_1 v_s + \Gamma_2 u + \Gamma_3 I_h. \quad (6)$$

Assuming that we have full control over u, a particle swarm optimization (PSO)-based state feedback controller is designed to ensure robustness under parametric variations. The control law is defined as

$$u_c = -K(z - z_{ref}) \quad (7)$$

Where z_{ref} is the desired state vector. An optimization function can be developed to find the optimal feedback gains to maximize the left shift and increase the damping ratio of the Eigen values of the state matrix given in (10). The optimization function is given as

$$minf = \sum_{i=1}^{N} [Re[\lambda_i(\Lambda_i - \Gamma_1 K)]] - \xi_i(\Lambda_i - \Gamma_1 K) \quad (8)$$

Subject to

$$K_{min1} < K_1 < K_{max1},\ K_{min2} < K_2 < K_{max2}$$

Subject to

$$K_{min1} < K_1 < K_{max1},\ K_{min2} < K_2 < K_{max2}$$

Here $K = [K_1\ K_2\ 0\ 0\ 0]$ and N is the number of possible operating conditions. K is the feedback controller gain vector having two nonzero elements. It is not possible to find the reference of the load current, so partial feedback is considered. Similarly, the feedback for the terminal voltage v_t and series capacitor voltage v_{cf} are considered to be zero, as they are dependent on the other network parameters (i_f and i_{sh}). Hence, only two feedback gains have been used. The terms λ_i and ξ_i in (11) are the critical eigenvalue and damping ratio of the state transition matrix ($\Lambda_i - \Gamma_{1i}\ K$) for i_{th} operating condition.

The optimization function (11) is formulated to find an optimal value of K, subjected to lower and upper bounds, to maximize the left shift of the real part of the critical eigenvalues and its damping ratio for each and every possible operating condition. PSO has been used to solve the optimization problem given in (11). The parameters for the PSO implementation. In this PSO implementation, 50 particles and 100 iterations are considered. The feedback gains are found to be K = [13.6759 6.5009 0 0 0].

IV. REFERENCE COMPENSATOR CURRENTS GENERATION

In this paper, the reference currents are generated using instantaneous symmetrical component theory and are given as

$$i^*_{fa} = i_{la} - i^*_{sa} = i_{la} - \frac{v_{ta}+\gamma(v_{tb}-v_{tc})}{\Delta}\left(P_{lavg} + P_{loss}\right)$$

$$i^*_{fb} = i_{lb} - i^*_{sb} = i_{lb} - \frac{v_{tb}+\gamma(v_{tc}-v_{ta})}{\Delta}\left(P_{lavg} + P_{loss}\right)$$

$$i^*_{fc} = i_{lc} - i^*_{sc} = i_{la} - \frac{v_{tc}+\gamma(v_{ta}-v_{tb})}{\Delta}\left(P_{lavg} + P_{loss}\right) \quad (9)$$

Where

$$\Delta = \sum_{j=a,b,c} v_{tj}^2, \gamma = \tan\varphi/\sqrt{3}..$$

Here, P_{lavg} is the average load power, P_{loss} denotes the switching losses and ohmic losses in actual compensator and it is generated using a capacitor voltage controller. The term P_{lavg} is obtained using a moving average filter of one cycle window of time T in seconds. The term is the desired phase angle between the source voltage and current.

In this paper, the load currents are unbalanced and distorted; these currents flow through the feeder impedance and make the voltage at PCC unbalanced and distorted. However, if the voltages are unbalanced and distorted, it is not possible to get balanced and sinusoidal currents after compensation using (13). To remove this limitation of the algorithm, fundamental positive sequence voltages $v^+_{ta1}(t)$, $v^+_{tb1}(t)$ and $v^+_{tc1}(t)$ of the distorted terminal voltages are extracted. Now, the voltages $v_{ta}(t)$,$v_{tb}(t)$, and $v_{tc}(t)$ in (13) are replaced by $v^+_{ta1}(t)$, $v^+_{tb1}(t)$, and $v^+_{tc1}(t)$, respectively. Therefore, the expressions for reference compensator currents become

$$i^*_{fa} = i_{la} - i^*_{sa} = i_{la} - \frac{v^+_{ta1}+\gamma(v^+_{tb1}-v^+_{tc1})}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)$$

$$i^*_{fb} = i_{lb} - i^*_{sb} = i_{lb} - \frac{v^+_{tb1}+\gamma(v^+_{tc1}-v^+_{ta1})}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right)$$

$$i^*_{fc} = i_{lc} - i^*_{sc} = i_{la} - \frac{v^+_{tc1}+\gamma(v^+_{ta1}-v^+_{tb1})}{\Delta^+_1}\left(P_{lavg} + P_{loss}\right) \quad (10)$$

Where

$$\Delta = \sum_{j=a,b,c}\left(v^+_{tj1}\right)^2, \gamma = \tan\varphi/\sqrt{3}.$$

The aforementioned algorithm gives balanced source currents after compensation irrespective of unbalanced and distorted supply.

The positive-sequence voltages that are extracted from the terminal voltages v_{ta} , v_{tb} , and v_{tc} are the reference filter capacitor voltages and are denoted by v^*_{sha} , v^*_{shb}, and v^*_{shc}. The reference filter capacitor currents are computed using these reference voltages and are given as follows:

$$\begin{bmatrix} i^*_{sha} \\ i^*_{shb} \\ i^*_{shc} \end{bmatrix} = \omega C_{sh} e^{j90} \begin{bmatrix} v^*_{sha} \\ v^*_{shb} \\ v^*_{shc} \end{bmatrix} \quad (15)$$

Once the reference quantities z_{ref} and the actual state vectors z are obtained from the measurements, the control signal for each phase is then computed using the reference and actual state vectors in the respective phases with the appropriate control gain K. The switching commands for the VSI switches are generated using the hysteresis band current control method. Hysteresis current controller schemes are based on a feedback loop, generally with two-level comparators. The switching commands (S_a, S'_a , S_b , S'_b , S_c , S'_c) are issued whenever the limit (*lim*) exceeds a specified tolerance band "±*h*." Unlike the predictive controllers, the hysteresis controller has the advantage of peak-current-limiting capacity apart from in addition to other merits such as extremely good dynamic performance, simplicity in implementation, and independence from load parameter variations. The disadvantage with this hysteresis method is that the converter switching frequency is highly dependent on the ac voltage and varies with it. The switching signals generated for the VSI are as follows:

$$u_c = -K(Z - Zref)$$

$$u = hys\left(-K\left(Z - Z_{ref}\right)\right). \quad (11)$$

If h ≥ lim then hys(h) = −1, bottom switch is turned ON, whereas top switch is turned OFF (Sa = 0, S'_a = 1).

If h ≤ lim then hys(h) = 1, top switch is turned ON, whereas bottom switch is turned OFF (Sa = 1, S'_a = 0).

The control circuitry is simple for both topologies because only three switching commands are to be generated. These three signals along with the complementary signals will control all the switches of the inverter.

V. SIMULATION RESULTS ANALYSIS

The table II represents the parameters of the system configuration. In order to validate the proposed topology, simulation is carried out using graphic-driven simulation software MATLAB. These gains are used to generate conventional topology. As the voltage across the inductor is

switching commands to the gates of the inverter as given in (16). The same system parameters that are given Table I with C_{sh} = 50 μF and C_f = 65 μF are used in MATLAB simulation. The simulation results for both the conventional topology and the proposed topology are presented in this section for better understanding and comparison between both the topologies.

TABLE I: SYSTEM PARAMETERS

System Quantities	**Values**
System Voltages	230 V (line to neutral), 50 Hz
Feeder impedance	Z_s=1+j3.141Ω
Linear load	Z_{la}=34+j47.5 Ω Z_{lb}=81+j39.6 Ω Z_{lc}=31.5+j70.9 Ω
Nonlinear load	Three phase full bridge rectifier load feeding a R-L load 150 Ω -300 mH
VSI parameters	C_{dc}=3300 μF, V_{dcref}=1.6V_m=520 V, L_f=26mH, R_f=0.1 Ω
Hysteresis band (h)	±0.5 A

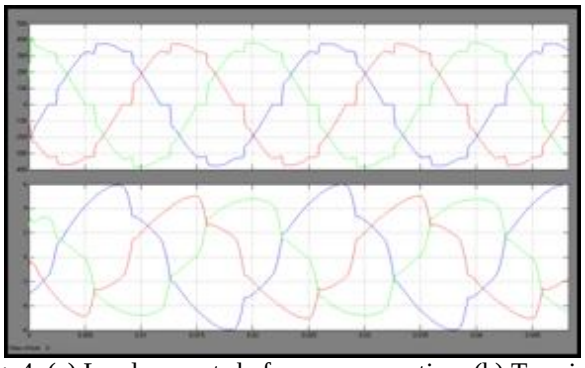
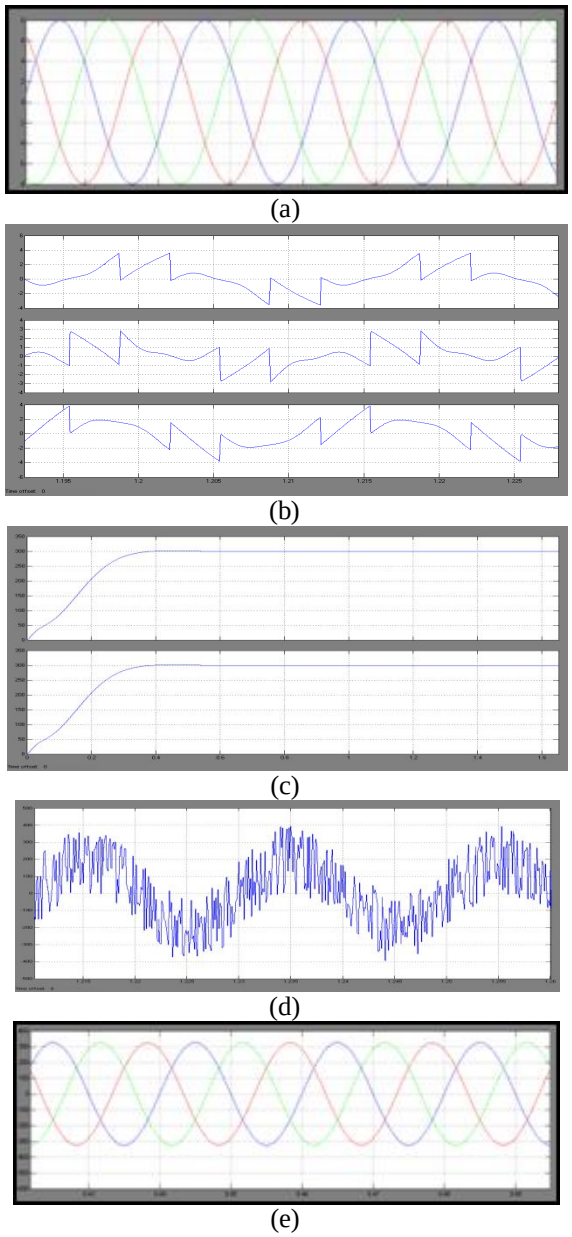


Fig. 4. (a) Load currents before compensation. (b) Terminal voltages before compensation.

The load currents and terminal (PCC) voltages before compensation are shown in Fig. 4. The load currents are unbalanced and distorted; the terminal voltages are also unbalanced and distorted because these load currents flow through the feeder impedance in the system. Fig.5 gives the simulation results of the DSTATCOM using the PI controlled VSI topology. The source currents after compensation are balanced and sinusoidal as shown in Fig. 5(a). These currents still contain the switching

frequency of the inverter. The three-phase compensator currents are depicted in Fig. 5(b). The dc link voltages across the top and bottom dc-link capacitors are shown in Fig. 5(c). The voltage across the inductor is shown in Fig. 5(d); the peak-to-peak voltage is 630 V, which is far lower than the voltage across the inductor using the high in case of the conventional topology, the rate of rise of filter current di_f/dt will be higher than that of the proposed topology. This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in proposed hybrid topology, the number of switchings will be less. Thus, the average switching frequency of the switches in the proposed topology will be less as compared to the conventional topology. Since the average switching is less, the switching loss will also decrease in the proposed topology. One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less.



as compared to the conventional DSTATCOM topology.

Fig. 5. Simulation results using proposed hybrid topology. (a) Source currents after compensation. (b) Filter currents. (c) DC capacitor voltages (top and bottom). (d) Voltage across the interfacing inductor in phase-*a*. (e) Terminal voltages after compensation.

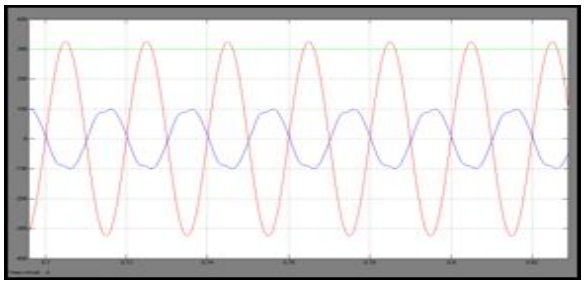


Fig. 6. Voltage across top dc capacitor, series filter capacitor, and terminal voltage in phase-*a*.

TABLE II: THD COMPARISIONS

THD %	Without compensation	Convent-ional	Propos-ed
Isa	11.10	1.48	0.70
Isb	12.48	1.59	0.78
Isc	13.63	1.95	1.36
Vta	7.32	3.52	0.43
Vtb	7.24	4.05	0.46
Vtc	7.46	3.51	1.01

This will improve the quality of compensation and total harmonic distortion (THD) will be less in the proposed topology. The terminal voltages after compensations are shown in Fig. 5(e),which are free from the switching freuzzquency components of the inverter. These switching frequency components are absorbed by the shunt capacitor by using state feedback control. The shunt capacitor provides a low impedance path at the high switching frequency. The THD of the source currents and terminal voltages before and after compensation in all the three phases are given in Table II.

VI. CONCLUSION

A new hybrid DSTATCOM topology has been proposed in this paper, which has the capability of compensating the load at a lower dc-link voltage under nonstiff source. Design of the Filter parameters is explained in detail. The proposed method Is validated through simulation and experimental studies in a 3-φ distribution system with the neutral clamped DSTATCOM Topology. From This study, it is found that the proposed topology has less average Switching frequency, less THDs in the source currents and Terminal voltages with reduced dc-link voltage

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